Signetics

Integrated circuits

Part 7 May 1981

Bipolar memories

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BIPOLAR MEMORY DATA MANUAL

1981

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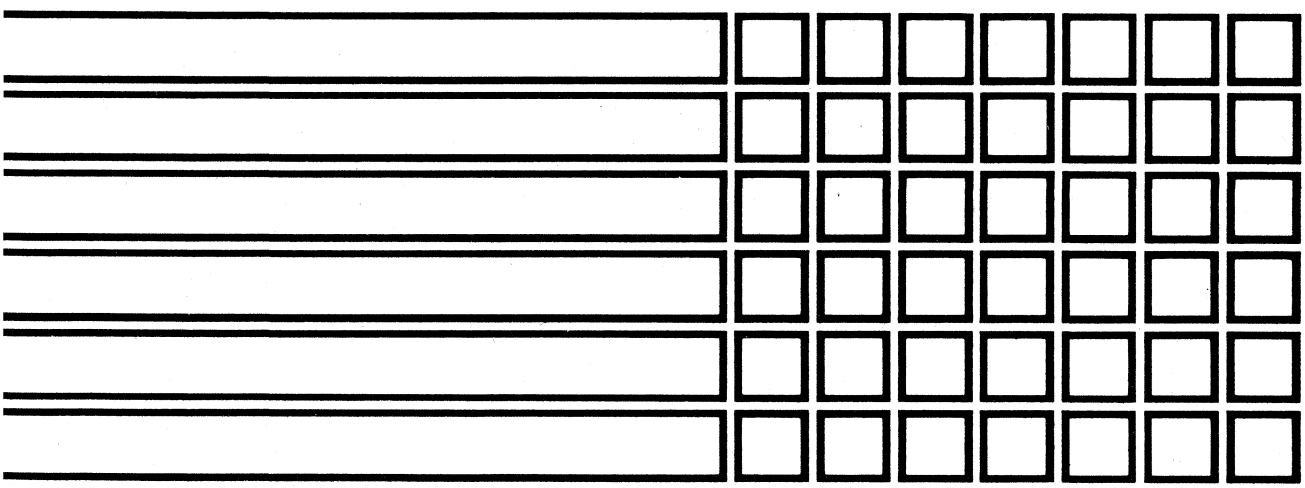

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INTRODUCTION

Rapid improvement in both the cost and performance of semiconductor memories has led to a dramatic increase in their usage in today's highly sophisticated electronic systems. Signetics has worked diligently over the last 16 years to develop the various technologies necessary to satisfy the broad range of users' semiconductor memory requirements.

Signetics offers a complete line of bipolar Schottky PROMs, programmable logic elements, RAM, and other special memory products for high speed applications. These products are available with organizations ranging from 64 to 2K bits for the RAM family and 256 to 16K bits for the PROM family. All Signetics' bipolar products are fabricated with double level metalization for maximum packaging density and low cost. PROM fuses are constructed with nichrome links for the highest reliability and programming yield in the industry. Signetics will continue to advance bipolar memory "state of the art" in 1981 with the introduction of new low power Schottky and latched PROMs, and other programmable array logic products.

The 1981 Signetics Memory Data Manual contains all necessary data on currently available products and those products which are planned for the future. In addition, the following pages provide product selection guides to aid the user in quickly selecting the optimum product for his particular system application.

Signetics reserves the right to make changes in the products contained in this book in order to improve design or performance and to supply the best possible products. Signetics also assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

BIPOLAR MEMORY CROSS REFERENCE*

AMD	SIGNETICS
2700	82S16
2701	82S17
27S02/3101A	3101A
54S289	82S25
27S08	82S23
27S09	82S123
27LS09	
27S12	82S130
27S13	82S131
27S15	82S115
27S20	82S126
27S21	82S129
27S29	82HS147
27S31	82S141
27S33	82S137
27S03	74S189
74S189	
27S180	82S180
27S181	82S181
27S185	82S185

FAIRCHILD	SIGNETICS
10415	10146
10416	10149
93403	82S25
93404	3101A
93405	74S189
93411	82S17
93417	82S126
93419	82S09
93421	82S16
93427	82S129
93431	82S23
93436	82S130
93446	82S131
93448	82S141
93453	82S137
93478	82S210
93479	82S212
93419	82S19
93450	82S180
93451	82S181
93L451	82LS181
93458	82S101
93459	82S100

NATIONAL	SIGNETICS
74S188	82S23
74S189	74S189
74S206	82S17
74S287	82S129
74S288	82S123
74S387	82S126
74S472	82HS147
74S570	82S130
74S571	82S131
74S573	82S137
85S181	82S181
85S180	82S180
87S296	82S141
54S289	82S25
82S185	82S185

MMI	SIGNETICS
5560	82S25
6300-1	82S126
6301-1	82S129
6305-1	82S130
6306-1	82S131
6330	82S23
6331	82S123
6341-1	82S141
6349	82HS147
6353-1	82S137
6380	82S180
6381	82S181
6530	82S17
6531	82S16
6560	3101A
6561	74S189
H6555	82S09
63S1681	82S191
PAL16R4	82S155†
PAL16R6	82S157†
PAL16R8	82S159†
PAL10H8	82S153†
PAL10L8	82S153†
PAL12H6	82S153†
PAL12L6	82S153†
PAL14H4	82S153†
PAL14L4	82S153†
PAL16H2	82S153†
PAL16L2	82S153†
PAL16L8	82S153†
PAL16C1	82S153†

INTEL	SIGNETICS
3101	82S25
3101A	3101A
3106	82S16
3107	82S17
3601	82S126
3602	82S130
3608	82S180
3621	82S129
3622	82S131
3624	82S141
3625	82S137
3628	82S181
3636	82S191

INTERSIL	SIGNETICS
5501	82S25
5523A	82S16
5533A	82S17
5600	82S23
5603A	82S126
5604	82S130
5610	82S123
5623A	82S129
5624	82S131
5625	82S141
56S26	82S137

MOTOROLA	SIGNETICS
4064	82S25
4256	82S16
5005	82S126
7641	82S141
7643	82S137
10139	10139
10149	10149
7680	82S180
7681	82S181
82100	82S100
82101	82S101

HARRIS	SIGNETICS
HM7602	82S23
HM7603	82S123
HM7610	82S126
HM7611	82S129
HM7620	82S130
HM7621	82S131
HM7625	82S114
HM7641	82S141
HM7643	82S137
HM7647	82S115
HM7649	82HS147
HM7680	82S180
HM7681	82S181
HM7681R	82S183
HM7685	82S185
HM76161	82S191

T.I.	SIGNETICS
54S289	82S25
74S188	82S23
74S189	74S189
74S287	82S129
74S288	82S123
74S289	3101A
74S387	82S126
74S472	82HS147
74S474	82S141
74S476	82S137
74S478	82S181
74S479	82S180
74S455	82S185
74LS478	82LS181

*Parts are pin for pin functional replacements except where noted. Signetics supplies most devices in both commercial and military temperature ranges.

†Parts are pin compatible and functionally equivalent with suitable program table translation. Open collector versions are also available.

BIPOLAR MEMORY SELECTION GUIDE

DEVICE	ORGANI-ZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME [ns][4]	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} [mA][4]
CAMs								
10155	8X2	OE	—	13	C	F,N	18	140
RAMs								
82S25	16X4	OC	B	50	M,C	F,N	16	105
3101A	16X4	OC	B	35	M,C	F,N	16	105
54/74S189	16X4	TS	B	35	M,C	F,N	16	110
82S21	32X2	OC	T	50	C	F,N	16	130
82S16	256X1	TS	T	50	M,C	F,N	16	115
82S17	256X1	OC	T	50	M,C	F,N	16	115
82S09	64X9	OC	T	45	M,C	I,N	28	190
82S19	64X9	OC	B	35	M,C	I,N	28	190
82S210*	256X9	TS	B	60	C	F,N	24	185
82S212*	256X9	TS	B	45	C	F	24	185
8X350*	256X8	TS	B	N/A	M,C	F	22	185
FPLAs								
82S100	16X48X8	TS	—	50	M,C	F,N	28	170
82S101	16X48X8	OC	—	50	M,C	F,N	28	170
82S152*	18X32X10	OC	I/O	40	M,C	F,N	20	155
82S155*	18X32X10	TS	I/O	40	M,C	F,N	20	155
FPGAs								
82S150*	18X12	OC	I/O	20	M,C	F,N	20	155
82S151*	18X12	TS	I/O	20	M,C	F,N	20	155
82S102	16X9	OC	—	35	M,C	F,N	28	170
82S103	16X9	TS	—	35	M,C	F,N	28	170
FPLSs								
82S104	16X48X8	OC	R	90	M,C	F,N	28	180
82S105	16X48X8	TS	R	90	M,C	F,N	28	180
82S154*	16X32X12	OC	I/O, R	65	M,C	F,N	20	155
82S155*	16X32X12	TS	I/O, R	65	M,C	F,N	20	155
82S156*	16X32X12	OC	I/O, R	65	M,C	F,N	20	155
82S157*	16X32X12	TS	I/O, R	65	M,C	F,N	20	155
82S158*	16X32X12	OC	I/O, R	65	M,C	F,N	20	155
82S159*	16X32X12	TS	I/O, R	65	M,C	F,N	20	155

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = 3-state
2. Output logic:
   T = Transparent—input data appears on output during Write
   B = Blanked—output is blanked during Write
   R = Output registers
   I/O = Input/Output option
3. Temperature range:
   C = Commercial (0°C to +75°C)
   M = Military (−55°C to +125°C)
   All ECL 10,000 series (−30°C to +85°C)
4. Commercial (0°C to +75°C)

BIPOLAR MEMORY SELECTION GUIDE (cont'd)

DEVICE	ORGANI-ZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME [ns][4]	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} [mA][4]
PROMs								
82S23	32X8	OC	—	50	M,C	F,N	16	77
82S123	32X8	TS	—	50	M,C	F,N	16	77
10139	32X8	OE	—	20	C	F,N	16	145
82S126	256X4	OC	—	50	M,C	F,N	16	120
82S129	256X4	TS	—	50	M,C	F,N	16	120
10149	256X4	OE	—	20	C	F	16	150
82S114	256X8	TS	—	60	M,C	F,N	24	175
82S130	512X4	OC	—	50	M,C	F,N	16	140
82S131	512X4	TS	—	50	M,C	F,N	16	140
82S115	512X8	TS	—	60	M,C	F,N	24	175
82S141	512X8	TS	—	60	M,C	F,N	24	175
	512X8	TS	—	45	C	F,N	20	155
82S137	1024X4	TS	—	60	M,C	F,N	18	140
	1024X4	TS	—	45	M,C	F,N	18	140
82LS181	1024X8	TS	—	175	M,C	F,N	24	80
82S180	1024X8	OC	—	70	M,C	F,N	24	175
82S181	1024X8	TS	—	70	M,C	F,N	24	175
	1024X8	TS	—	70	M,C	F,N	24	185
82S183	1024X8	TS	—	60	M,C	F,N	24	175
82S2708	1024X8	TS	—	225	M	F	24	85
82S185	2048X4	TS	—	100	M,C	I,N	18	120
	2048X4	TS	—	70	M,C	I,N	18	120
82S191	2048X8	TS	—	60	M,C	F,N	24	175
	2048X8	TS	—	80	M,C	I,N	24	175

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = 3-state
2. Output logic:
   T = Transparent—input data appears on output during Write
   B = Blanked—output is blanked during Write
   R = Output logic
   I/O = Input/output option
3. Temperature range:
   C = Commercial (0°C to +75°C)
   M = Military (−55°C to +125°C)
   All ECL 10,000 series (−30°C to +85°C)
4. Commercial (0°C to +75°C)

BIPOLAR MEMORY DATA SPECIFICATIONS

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DESCRIPTION

The 10155 is a 16-bit ECL Content Addressable Memory (CAM) organized as an array of 8 words by 2 bits. Each cell of the array consists of a D-type latch and an exclusive-OR comparator, along with control logic for reading, writing and masking.

The modes of operation possible with the 10155 are associate, masked associate, read, write, and hybrid. Lines Y_0-Y_7 are used for linear word select in the read/write mode, and are used as outputs for match/mismatch information in the associate mode.

In associate operation, I_0 and I_1contain information to be compared. If the latches at a particular Y location are in a state matching the input data, that Y line goes low.

The Y outputs are open emitters, allowing expansion in multiples of 2 bits by tying additional 10155's to the Y bus lines. To inhibit comparison of a particular bit, the corresponding A_0 or A_1 line is held low.

In the read mode, the state of the selected cells appears on outputs D_0 and D_1. In the write mode, these outputs are transparent, following the state of I_0 and I_1.

In Hybrid mode, one of the I_0 or I_1 data inputs may be associated with the Q_{n0} or Q_{n1} cells respectively. If a match exists, the corresponding Y_n line(s) will go low, and can be used to address the other half of the memory for writing new data. Thus, it is possible to write I_1 in Q_{n1} where I_0 matches Q_{n0} or vice versa.

FEATURES

- **12ns associate time (max.)**
- **Linear address select**
- **Single bit masking**
- **50 Ω output drive**
- **ECL 10K compatible**
- **Open emitter match lines for easy bit expansion**
- **50kΩ input pulldown resistors (except on Y lines)**

APPLICATION

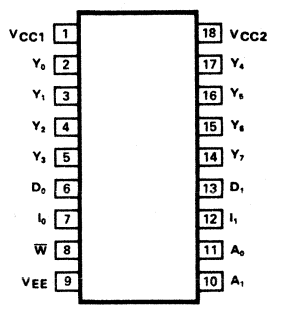
- **Content addressable memory systems**

RECOMMENDED OPERATING VOLTAGES

- $V_{CC1} = V_{CC2} = 0V$
- $V_{EE} = -5.2V \pm 5\%$

PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic

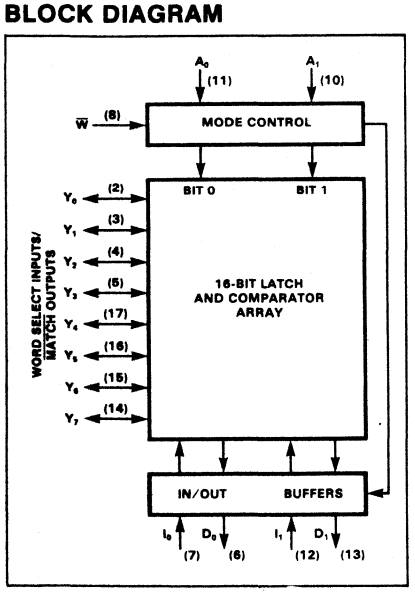
TRUTH TABLE (POSITIVE LOGIC)

MODE	A_0	A_1	I_0	I_1	$\overline{W}$	D_0	D_1	Q_{n0}	Q_{n1}	Y_n
Associate[1]	1	1	1/0	1/0	X	0	0	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0 + Q_{n1} \oplus I_1$
Associate[1,2] (masked)	1	0	1/0	X	1	0	D_1	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0$
Associate[1,2] (masked)	0	1	X	1/0	1	D_0	0	Q_{n0}	Q_{n1}	$Q_{n1} \oplus I_1$
Read[3]	0	0	X	X	1	D_0[2]	D_1[2]	Q_{n0}	Q_{n1}	0 (Selected address)
Write[3,4]	0	0	1/0	1/0	0	I_0	I_1	I_0	I_1	0 (Selected address)
Hybrid[5]	1	0	1/0	1/0	0	0	I_1	Q_{n0}	$I_1 \cdot \overline{Y_n}$	$Q_{n0} \oplus I_0$
Hybrid[5]	0	1	1/0	1/0	0	I_1	0	$I_0 \cdot \overline{Y_n}$	Q_{n1}	$Q_{n1} \oplus I_1$

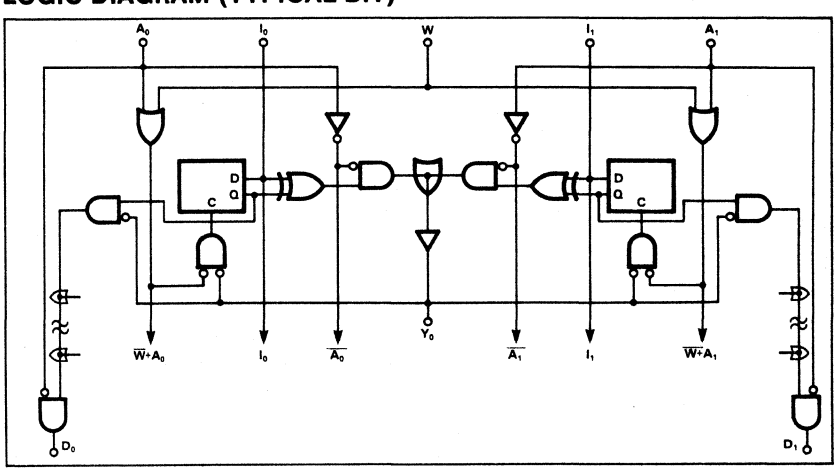
X = Don't care
Q_{n0} = Contents of address n, Bit 0 (n = 0 to 7)
Q_{n1} = Contents of address n, Bit 1

NOTES
1. 1 (high) = Mismatch, 0 (low) = Match
2. Read mode: $D_0 = Q_{00} \cdot \overline{Y_0} + Q_{10} \cdot \overline{Y_1} + \cdots + Q_{70} \cdot \overline{Y_7}$
   $D_1 = Q_{01} \cdot \overline{Y_0} + Q_{11} \cdot \overline{Y_1} \cdots + Q_{71} \cdot \overline{Y_7}$
3. In normal operation a single Y address is selected for read or write
4. Write is transparent
5. Simultaneous Associate and Write at all "Match" addresses.

BLOCK DIAGRAM



LOGIC DIAGRAM (TYPICAL BIT)



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2} = 0V$

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	-8	Vdc
V_{IN}	Input voltage	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature Range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

DC ELECTRICAL CHARACTERISTICS[1] $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER		TEST CONDITIONS	-30 °C			+25 °C			+85 °C			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Input voltage											V
V_{IL}	Low		-1.890			-1.850			-1.825			
V_{IH}	High				-0.890			-0.810			-0.700	
V_{ILA}	Low threshold				-1.500			-1.475			-1.440	
V_{IHA}	High threshold		-1.205			-1.105			-1.035			
	Output voltage											V
V_{OL}	Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.65		-1.85	-1.825		-1.615	
V_{OH}	High		-1.06		-0.89	-0.96		-0.81	-0.89		-0.70	
V_{OLA}	Low threshold				-1.655			-1.63			-1.595	
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	-1.08			-0.98			-0.91			
	Input current											μA
I_{IL}	Low	A,I,W = V_{IL} Min				0.5						
I_{IH}	High	A = V_{IH} Max						220				
		I,W = V_{IH} Max						200				
		Y = V_{IH} Max						50				
I_{EE}	Supply current	V_{IH} Max						140				mA

AC ELECTRICAL CHARACTERISTICS[2] $-30°C \le T_A \le +85°C$, $V_{CC1} = V_{CC2} = +2V$, $V_{EE} = -3.2V$, $R_L = 50\Omega$ to ground

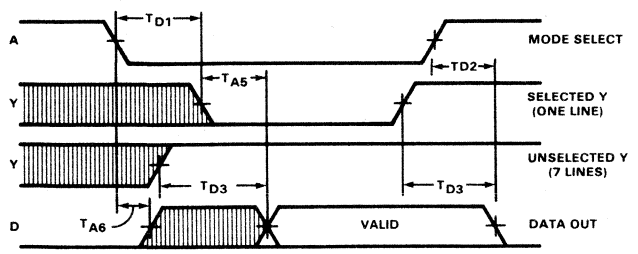
PARAMETER		FROM	TO	TEST CONDITIONS	LIMITS			UNIT
					Min[3]	Typ	Max	
	Associate time							ns
T_{A1}		I±	Y±				12	
T_{A2}		A+	Y+				12	
	Disable time							ns
T_{D1}		A-	Y-				12	
T_{D2}		A+	D-				7	
T_{D3}		Y+	D-				13	
	Setup and hold time							ns
T_{H1}	Hold time	$\overline{W}$+	A+		1			
T_{S2}	Setup time	A-	Y-		15			
T_{H2}	Hold time	$\overline{W}$+	Y±		3			
T_{S3}	Setup time	Y+	$\overline{W}$-		3			
T_{H3}	Hold time	$\overline{W}$+	I±		3			
T_{S4}	Setup time	I±	$\overline{W}$+		5			
T_W	Write pulse width				10			ns
	Access time							ns
T_{A3}	Write	$\overline{W}$-	D±	$T_{S4} \ge T_W$			17	
T_{A4}	Write	I+,-	D+,-				13	
T_{A5}	Read	Y-	D+				10	
T_{A6}	Read	A-	D+					

NOTES

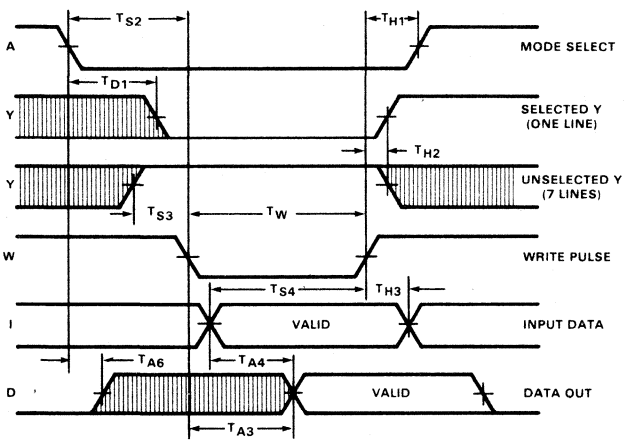
1. Each ECL 10K series device has been designed to meet the dc and ac specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
2. Refer to dc characteristics.
3. Minimum allowed.

VOLTAGE WAVEFORMS

READ CYCLE

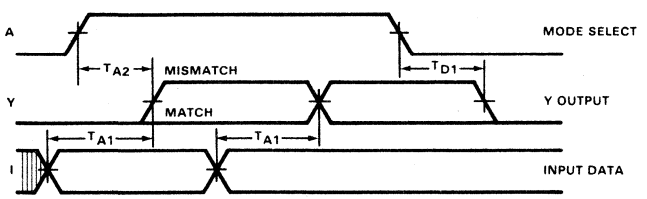


WRITE CYCLE

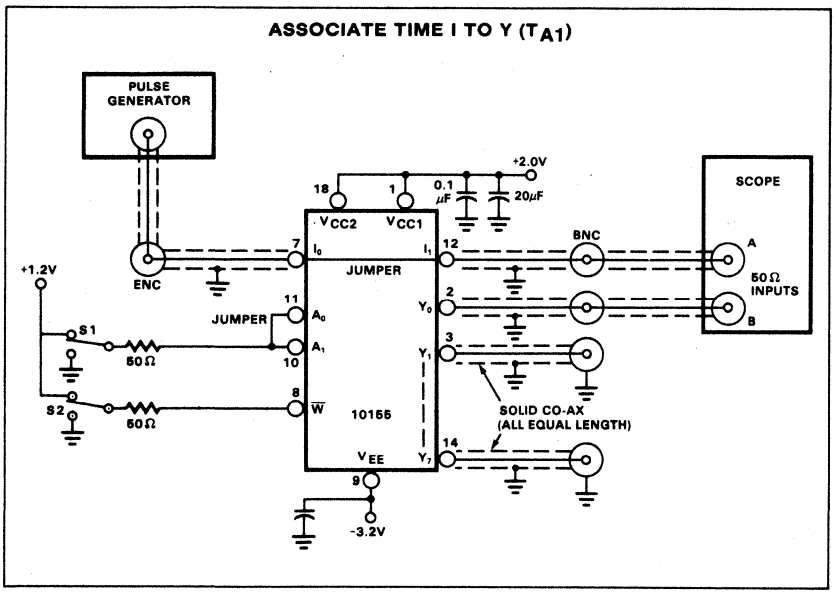


NOTE:
Only one word is shown selected but no restriction exists i.e., any number of addresses 0 to 8 may be written simultaneously.

ASSOCIATE CYCLE



MEASUREMENT CIRCUIT



82S25-F,N • 3101A-F,N,W • 54/74S189-F,N,W

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N74S189N, N82S25N, and for the military temperature range (-55°C to +125°C) specify S54S189 F or W, S82S25 F or W.

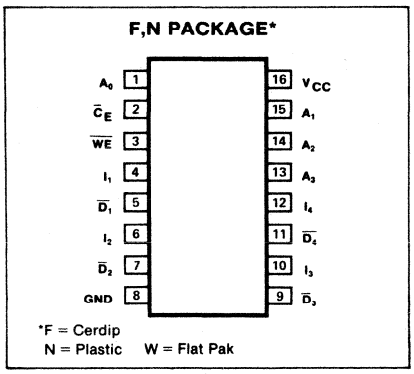
FEATURES

- **Output access time:**
  N82S25: 50ns max
  N3101A: 35ns max
  N74S189: 35ns max
  S54S189: 50ns max
- **Power dissipation: 6.25mW/bit, typ**
- **Input loading:**
  N grade: -100μA max
  S grade: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S25: Open collector
  3101A: Open collector
  54/74S189: Tri-state
- **Schottky processed**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

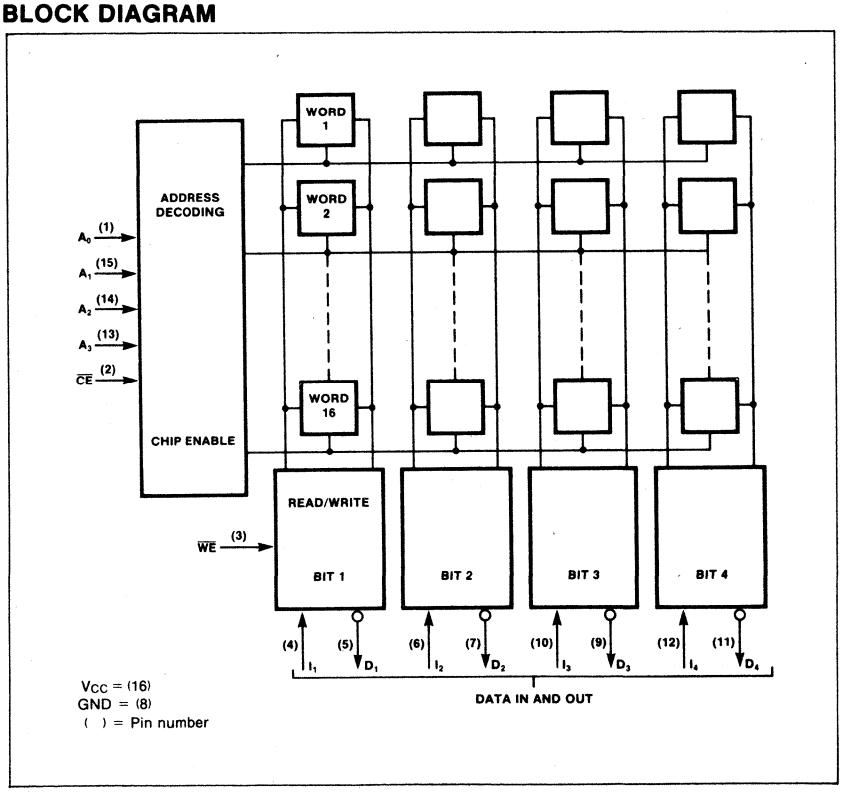
PIN CONFIGURATION



TRUTH TABLE

	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	54/74S189
				DATA OUT		
Read	0	1	X	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

BLOCK DIAGRAM



AC ELECTRICAL CHARACTERISTICS

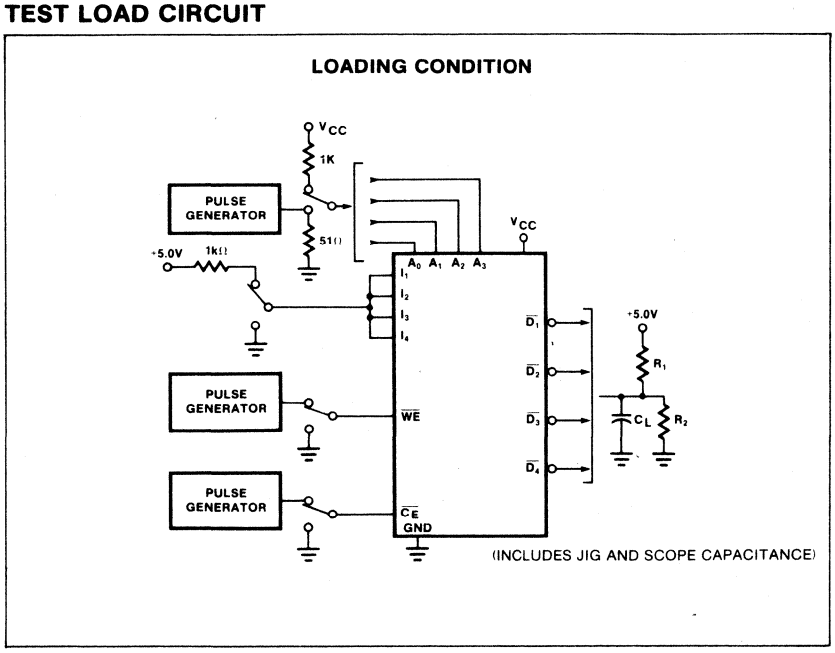
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $-55°C \le T_A \le +125°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	N82S25			S82S25			N3101A, N74S189			S54S189			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Access time															ns
T_{AA}	Address					50			60			35			50	
T_{CE}	Chip enable					35			35			17			25	
T_{CD}	Disable time	Output	Chip enable			35			35			17			40	ns
T_{WD}	Response time	Output	Write enable			25			30			25			50	ns
T_{WR}	Write recovery time					50			60			35			40	ns
	Setup and hold time															ns
T_{WSA}	Setup time	Write	Address	5			10			0			0			
T_{WHA}	Hold time	enable		5			10			0			10			
T_{WSD}	Setup time	Write	Data in	30			30			25			30			
T_{WHD}	Hold time	enable		5			10			0			10			
T_{WSC}	Setup time	Write	$\overline{CE}$	0			0			0			0			
T_{WHC}	Hold time	enable		5			5			0			0			
	Pulse width															ns
T_{WP}	Write enable[5]			30			30			25			30			

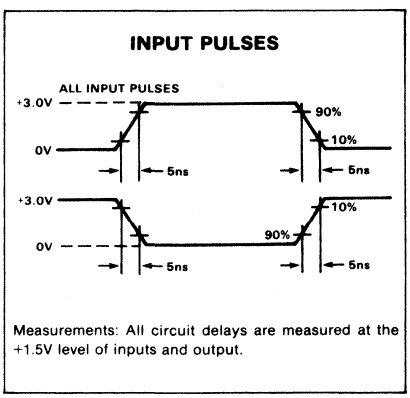
NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: high ≈ +5.0V, low ≈ GND.
7. Test each input one at a time.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage High	+5.5	Vdc
T_A	Temperature range Operating		°C
	N grade	0 to +75	
	S grade	-55 to +125	
T_{STG}	Storage	-65 to +150	

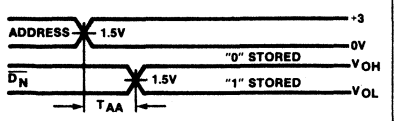
DC ELECTRICAL CHARACTERISTICS

N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[7]		TEST CONDITIONS[6]	N GRADE			S GRADE			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,7]	I_{IN} = -12mA, V_{CC} = Min			-1.5			-1.5	
	Output voltage	$\overline{CE}$ = Low							V
V_{OL}	Low[2,3,1]	I_{OUT} = 16mA, V_{CC} = Min			0.45			0.5	
V_{OH}	High (54/74S189)[1]	I_{OUT} = 2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			10			25	
	Output current								
I_{OLK}	Leakage	$\overline{CE}$ = high, V_{OUT} = 5.5V, V_{CC} = Min			100			100	μA
I_{OS}	Short circuit (54/74S189)	$\overline{CE}$ = Low V_{OUT} = 0V			-100	-30		-100	mA
$I_{O(OFF)}$	Hi-Z (54/74S189)	$2.4 \ge V_{OUT} \ge 0.4V$			±50			±50	μA
I_{CC}	Supply current[3]								mA
	82S25				105			120	
	3101A				105			120	
	54/74S189				110			110	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V, $\overline{CE}$ = high		8			8		

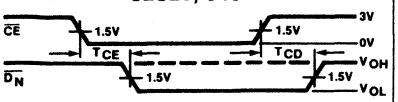
TIMING DIAGRAMS

READ CYCLE



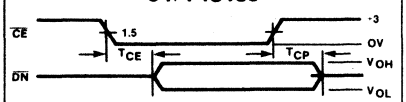
Address Access Time

82S25, 3101A



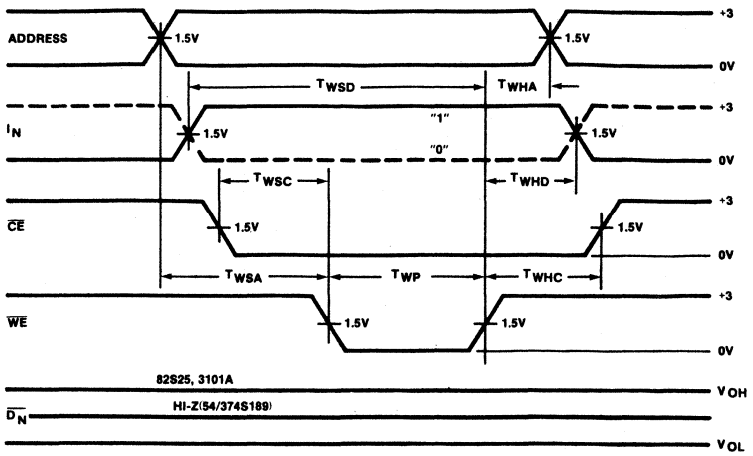
Chip Enable/Disable Times
Open Collector

54/74S189



Chip Enable/Disable Times
Tri-State

WRITE CYCLE



82S21-F,N

DESCRIPTION

The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5-input decoder when the chip enable input, CE is at logic high. $\overline{WS_0}$ and $\overline{WS_1}$ are the write select inputs for the bit 0 and bit 1 of the word selected. $\overline{WE}$ is the write control input. When $\overline{WS_N}$ and $\overline{WE}$ are both at logic low data on the DI_0 and DI_1 data lines are written into the addressed word. The read function is enabled when either $\overline{WS_N}$ or $\overline{WE}$ is at logic high.

An internal latch provides the Write-While-Read capability. When the latch control line (strobe) is logic high and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When strobe goes from a logic high to logic low, the outputs are latched and will remain latched regardless of the state of any other address or control line. When strobe goes from low to high, the outputs unlatch and will assume the contents of the present address word.

FEATURES

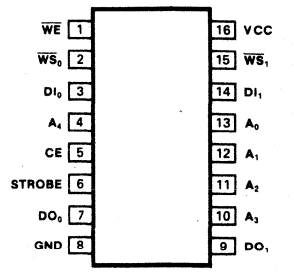
- **Address access time: 50ns max**
- **Write cycle time:**
  Transparent mode: 45ns max
  Latched mode: 60ns max
- **Power dissipation: 7.5mW/bit typ**
- **32mA output sink capability**
- **On-chip output latches**
- **Bit masking control lines**
- **Write-While-Read function**
- **Non-inverting open collector outputs**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Accumulator register**
- **Control store**

PIN CONFIGURATION

F,N PACKAGE



*F = Cerdip
N = Plastic

TRUTH TABLE

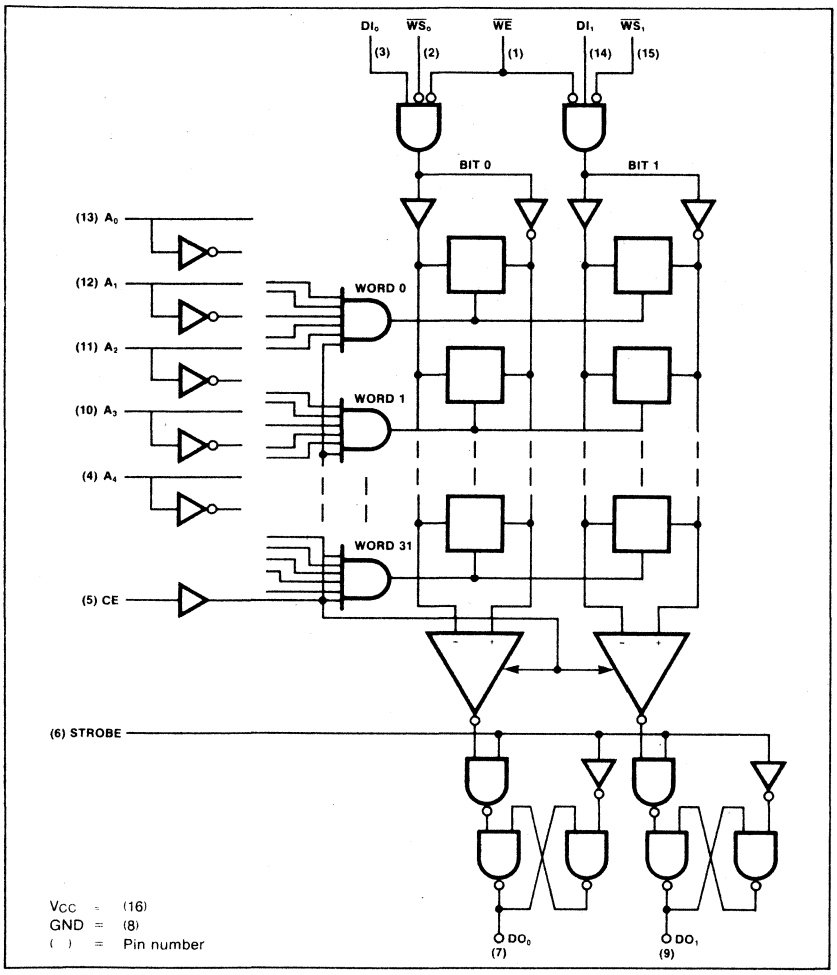
CE	$\overline{WE}$	$\overline{WS_0}$	$\overline{WS_1}$	STROBE	MODE	OUTPUTS
X	X	X	X	0	Output hold	$DO_N = (A_M)$ at last CE = high
0	X	X	X	0	Disabled	DO_N = high
1	1	X	X	1 or ↓	Read (transparent/latched)	$DO_N = (A_M)$
1	0	1	1	1 or ↓	Read (transparent/latched)	
1	0	0	0	0	Write data	$DO_N = (A_M)$ at last strobe = ↓
1	0	0	0	1	Write data	$DO_N = DI_N$
1	0	0	1	X	Write data into bit 0 only	If strobe = low: $DO_N = (A_M)$ at last strobe = ↓ If strobe = high: $DO_N = DI_N$ or (A_M) as per $\overline{WS_N}$
1	0	1	0	X	Write data into bit 1 only	

( ) = Contents of
↓ = High to low transition

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage	+5.5	Vdc
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER[1]		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = 4.75V			0.85	
V_{IH}	High[1]	V_{CC} =5.25V	2			
V_{IC}	Clamp[1,2]	V_{CC} = 4.75V, I_{IN} = -18mA			-1.2	
	Output voltage					V
V_{OL}	Low[1,3]	V_{CC} = 4.75V, I_{OL} = 32mA			0.45	
	Input current					
I_{IL}	Low	V_{IN} = 0.45V			-1.6	mA
I_{IH}	High	V_{IN} = 5.5V			25	μA
	Output current	V_{CC} = 5.25V				μA
I_{OLK}	Leakage[4]	V_{OUT} = 5.25V			40	
I_{CC}	V_{CC} supply current[5]	V_{CC} = 5.25V			130	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$, $R_1 = 150\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Access time							ns
T_{AA} Address	Output	Address	Latched or transparent read			50	
T_{CE} Chip enable	Output	Chip enable				50	
Disable time							ns
T_{CD} Chip enable	Output	Chip enable	Latched or transparent read			50	
Setup and hold time							ns
T_{WSA} Setup time	Write	Address	Latched or transparent write	15			
T_{WHA} Hold time				5			
T_{WSD} Setup time	Write	Data in	Latched or transparent write	25			
T_{WHD} Hold time				5			
T_{WSC} Setup time	Write	CE	Latched or transparent write	15			
T_{WHC} Hold time				5			
T_{CES} Setup time	Strobe	Chip enable	Latched read	50			
T_{CEH} Hold time				5			
T_{ADH} Hold time	Output	Address	Latched read	5			
Pulse width							ns
T_{SW} Strobe			Latched read	30			
T_{WP} Write inputs			Latched or transparent write	25			
Latch time							ns
T_{SLR} Read strobe	Strobe	Address	Latched read	50			
T_{SLW} Write strobe	Strobe	Write	Latched write	40			
T_{LRW} WWR strobe	Write	Strobe	Write while read	10			
Delatch time							ns
T_{DL} Strobe	Output	Strobe	Latched read			25	
T_{WD} Valid time	Output	Write	Latched or transparent write			40	ns

NOTES
1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
4. Measured with V_{IL} applied to CE, and V_{IH} to strobe.
5. I_{CC} is measured with all inputs at 4.5V, and the outputs open.

MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable high (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes low and Data Output is in high state.

T_{AA} Delay between beginning of valid Address (with Chip Enable high) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output reflects the contents of the Data Input.

T_{CES} Minimum delay between leading edge of Chip Enable and trailing edge of Strobe, for latching valid output data.

T_{CEH} Required delay between trailing edge of Strobe and end of Chip Enable, for latching valid output data.

T_{SLR} Minimum delay between Address valid time and trailing edge of Strobe, for latching valid output data.

T_{SW} Minimum width of Strobe pulse required to update contents of output data latches.

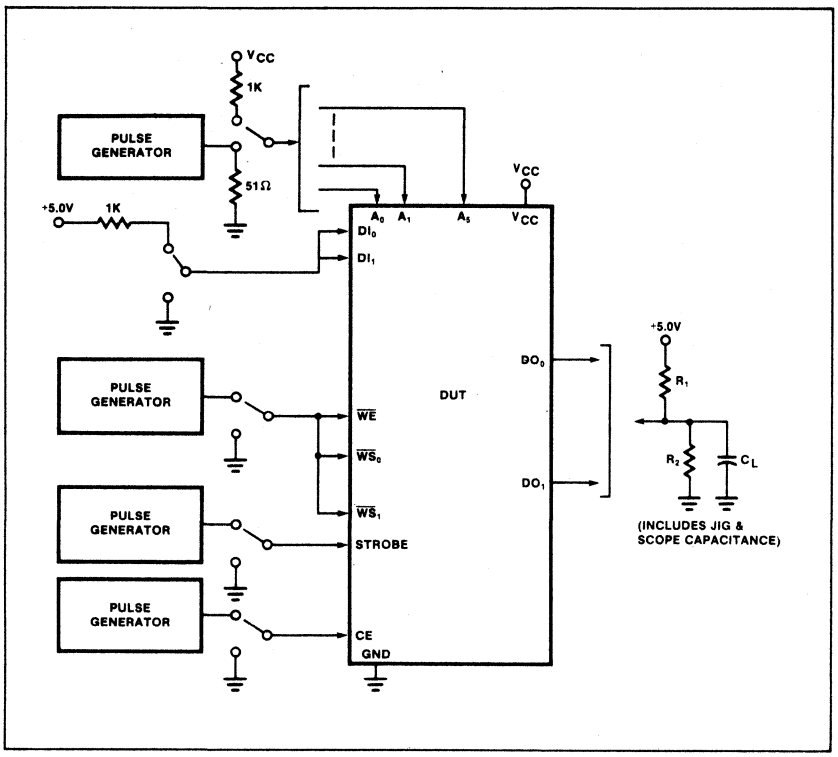
T_{ADH} Required delay between trailing edge of Strobe and end of valid Address.

T_{DL} Delay between leading edge of Strobe and when output data latches are released.

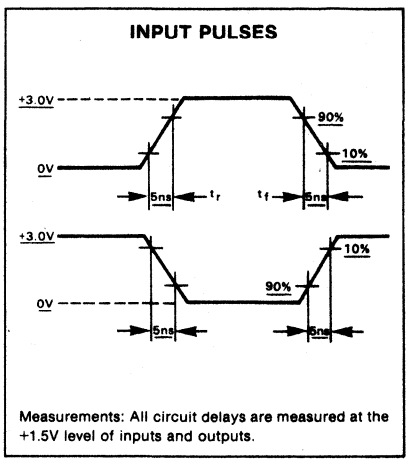
T_{LRW} Minimum delay required between trailing edge of Strobe and leading edges of Write Enable or Write Select for latching old output data (being read) while new data is being written (at the same address).

T_{SLW} Minimum delay between leading edge of Write Enable or Write Select and trailing edge of Strobe for latching data being written in output data latches.

TEST LOAD CIRCUIT

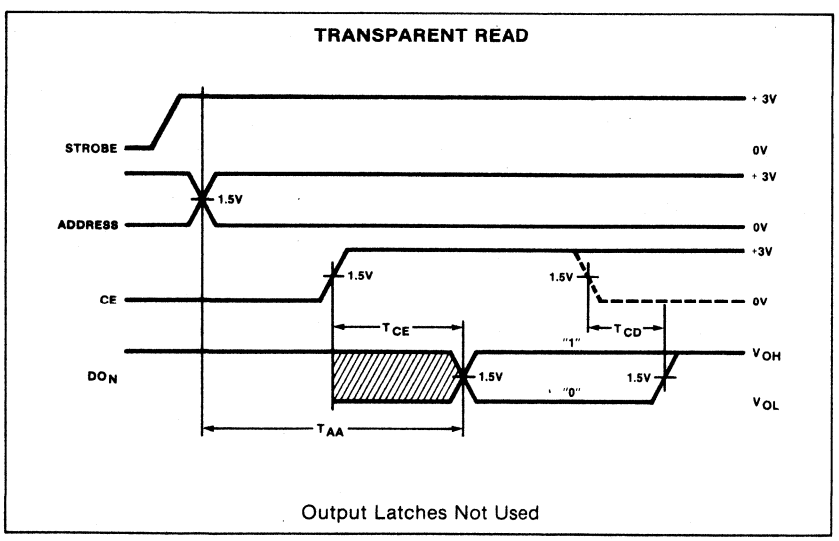


VOLTAGE WAVEFORM



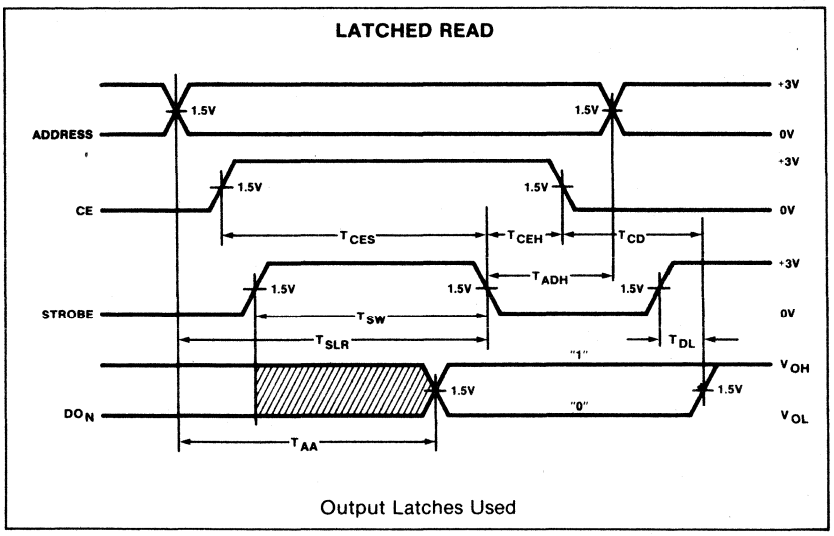
Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAMS

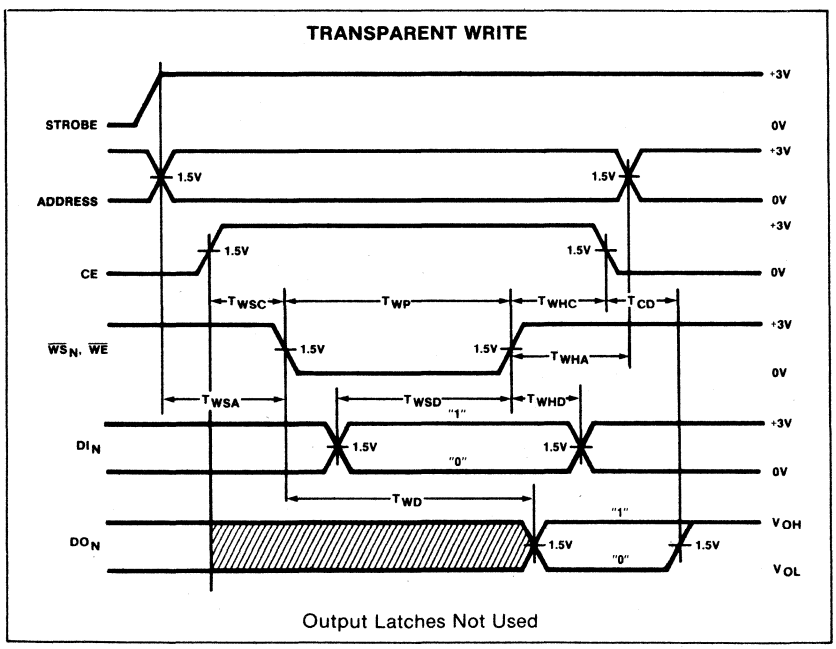


Output Latches Not Used

TIMING DIAGRAMS (Cont'd)



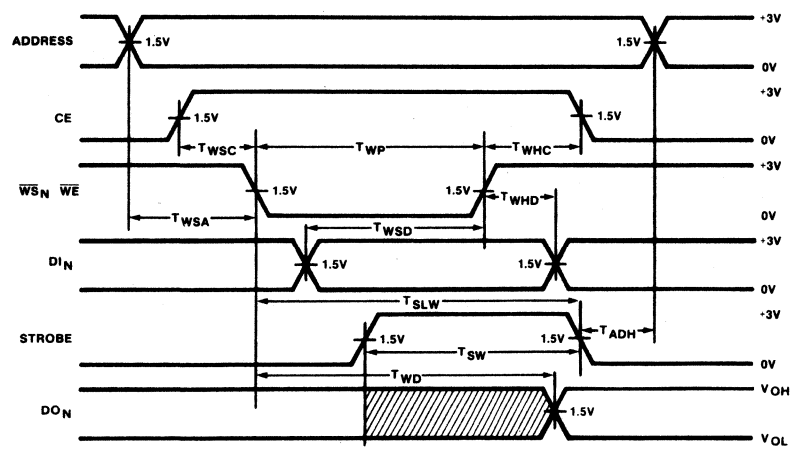
Output Latches Used



Output Latches Not Used

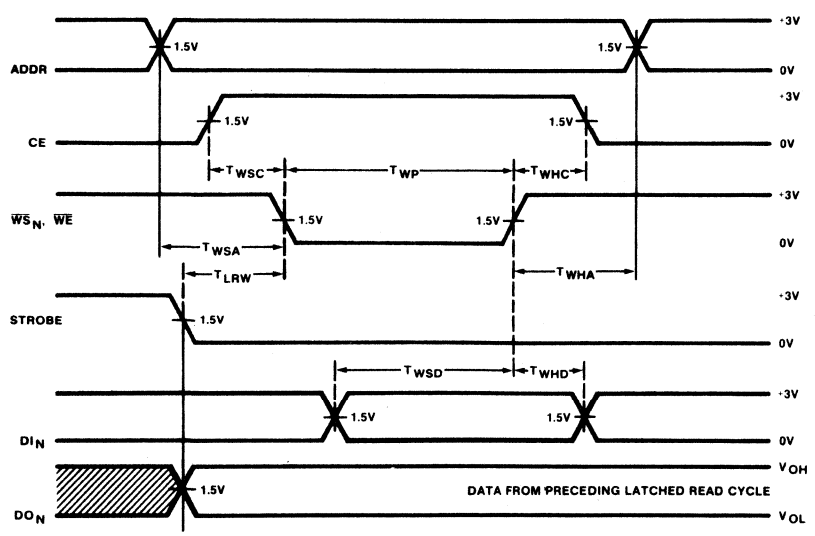
TIMING DIAGRAMS (Cont'd)

LATCHED WRITE



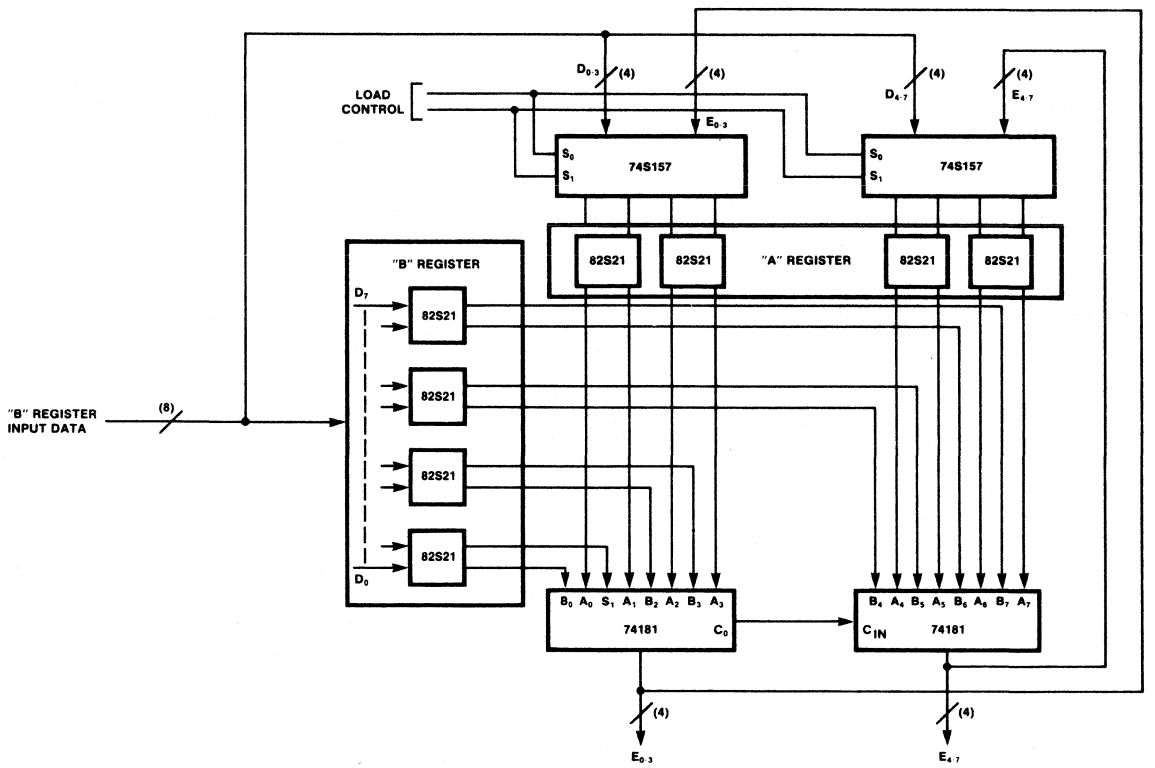
Output Latches Used

WRITE-WHILE-READ



TYPICAL APPLICATION

BASIC 8-BIT FULLY BUFFERED ACCUMULATOR



By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32X8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

DESCRIPTION

The 54/74S301 is a read/write memory array which features an open collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors, which reduces input loading to 25μA for a high level and -250μA (S54S301) or -250μA (N74S301) for a low level.

The additional feature of output blanking during Write ($\overline{D}_O$ terminal "H") permits $\overline{D}_O$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast read access and write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

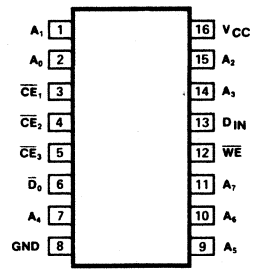
The 54/74S301 is available in both the commercial and military temperature ranges. The commercial temperature range (0°C to +75°C) is specified as N74S301, F or N, and the military temperature range (−55°C to +125°C) is specified as S54S301, F only.

FEATURES

- **Address access time:**
  N74S301: 50ns max
  S54S301: 70ns max
- **Write cycle time:**
  N74S301: 50ns max
  S54S301: 60ns max
- **Power dissipation : 1.5mW/bit typ**
- **Input loading:**
  N74S301: -100μA max
  S54S301: -250μA max
- **Output blanking during Write**
- **On-chip address decoding**
- **Output option:**
  54/74S301: Open collector
- **Schottky clamped**
- **TTL compatible**

PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic

APPLICATIONS

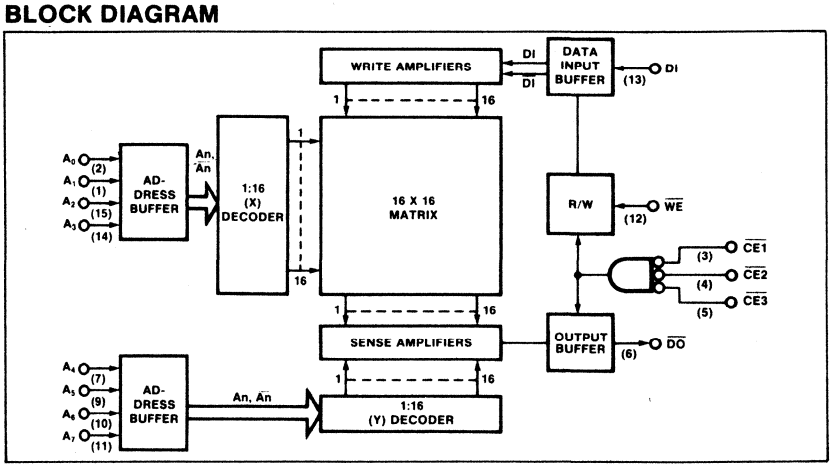
- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$ 54/74S301
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OUT}	High (54/74S301)	+5.5	
	Temperature range		°C
T_A	Operating		
	N74S301	0 to +70	
	S54S301	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N74S301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$

S54S301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N74S301			S54S301			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,2]	V_{CC} = Min, I_{IN} = -18mA			-1.2			-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,3]	I_{OL} = 16mA			0.45			0.50	
	Input current[2]	V_{CC} = Max							
I_I	At V_{IN} Max	V_{IN} = 5.5V			1			1	mA
I_{IL}	Low	V_{IL} = 0.45V			-100			-250	μA
I_{IH}	High	V_{IH} = 2.7V			25			25	μA
	Output current								
I_{OLK}	Leakage[4]	V_{IH} = 2V, V_O = 5.5V			40			50	μA
I_{CC}	V_{CC} supply current[5]	V_{CC}= Max			130			130	mA
		V_{CC} = Max, T_A = +125°C						99	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

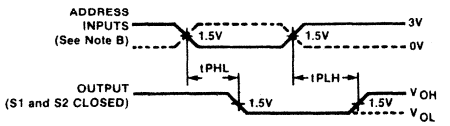
(Cont'd) $R_L = 270\Omega$, $C_L = 15pF$, See ac test load
N74S301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$
S54S301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[6]		TO	FROM	TEST CONDITIONS	N74S301			S54S301			UNIT
					Min	Typ	Max	Min	Typ	Max	
	Access time [B,D,E]										ns
t_{PLH}	Low to high		Address								
t_{PHL}	High to low										
t_{PLH}	Low to high		Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			50			70	
	Enable time										ns
t_{ZL}	Low [C,D,F,G]	Output	Chip enable								
t_{ZH}	High [C,D,F,G]										
t_{PHL}	High to low [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			35			45	
	Disable time										ns
t_{LZ}	Low [C,D,F,G]	Output	Chip enable	$C_L=5pF$							
t_{HZ}	High [C,D,F,G]										
t_{PLH}	Low to high [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			20			30	
t_{PHL}	High to low [C,D,E]		Write enable				30			40	
t_{LZ}	Low [D,G]	Output	Write enable	$C_L=5pF$							
t_{HZ}	High [D,G]										
	Sense recovery time										ns
t_{ZL}	Low [D,F]										
t_{ZH}	High [D,F]										
t_{SR}	Sense [D]						40			50	
	Pulse width [H]										ns
t_W	Write enable			$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
	Setup and hold time [D]										ns
t_S	Setup time	Write enable	Address								
t_H	Hold time	Address	Write enable								
t_S	Setup time	Write enable	Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Address	Write enable		10			10			
t_S	Setup time	Write enable	Data								
t_H	Hold time	Data	Write enable								
t_S	Setup time	Write enable	Data	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
t_H	Hold time	Data	Write enable		10			10			
t_S	Setup time	Write enable	Chip enable								
t_H	Hold time	Chip enable	Write enable								
t_S	Setup time	Write enable	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Chip enable	Write enable		0			0			

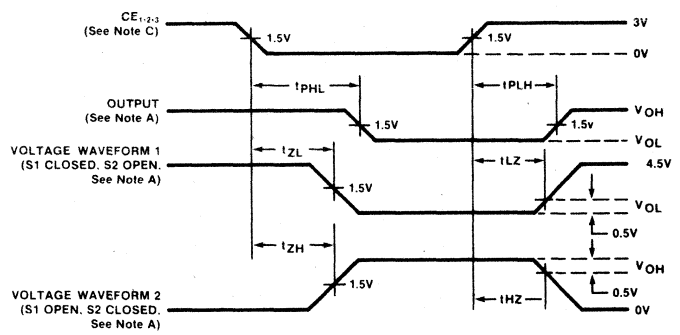
NOTES
1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
5. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
6. See timing diagram notes.

TIMING DIAGRAMS

READ CYCLE

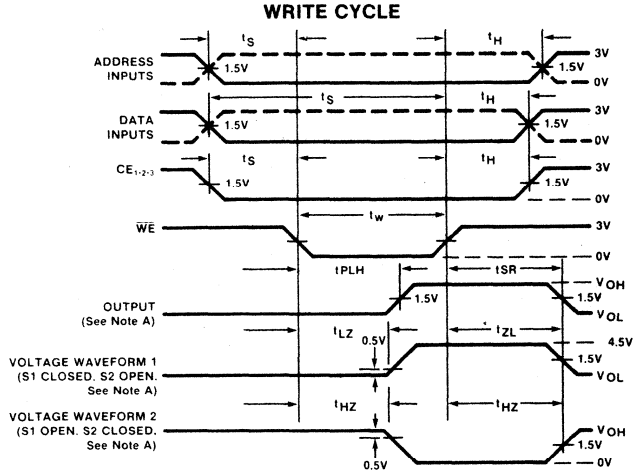


Access Time From Address



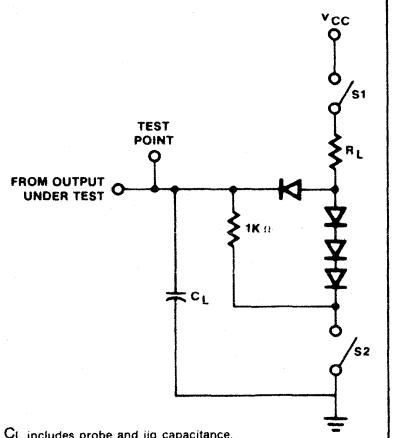
Chip Enable and Disable Time

WRITE CYCLE



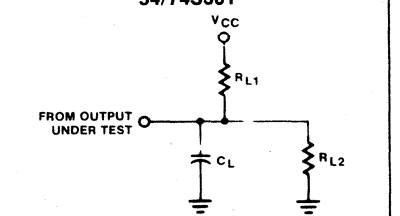
TEST LOAD CIRCUITS

54/74S200/201



CL includes probe and jig capacitance.
All diodes are 1N3064.

54/74S301



CL includes probe and jig capacitance.
All diodes are 1N3064

NOTES

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ns, $t_f \leq 2.5$ns, PRR ≤ 1MHz, and $Z_{OUT} \approx 50\Omega$.
E. t_{PLH} propagation delay time, low-to-high level output, t_{PHL} propagation delay time, high-to-low level output.
F. t_{ZH} propagation delay time, Hi-Z to high level output, t_{ZL} propagation delay time, Hi-Z to low level output.
G. T_{HZ} propagation delay time, high level to Hi-Z output, t_{LZ} propagation delay time, low level to Hi-Z output.
H. Minimum required to guarantee a Write into the slowest bit.

DESCRIPTION

The 82S16 is a read/write memory array which features tri-state output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors which reduce input loading to 25μA for a high level, and −100μA for a low level.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

The device has a fast read access and write cycle time, and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

The 82S16 is available in the commercial temperature range (0°C to +75°C) and are specified as N82S16, F or N. The 82S16 is also available in the military temperature range (−55°C to +125°C) and is specified as S82S16.

FEATURES

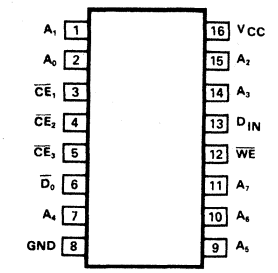
- **Address access time:**
  N82S16: 50ns max
  S82S16: 70ns max
- **Write cycle time:**
  N82S16: 40ns max
  S82S16: 55ns max
- **Power dissipation: 1.5mW/bit typ**
- **Input loading:**
  N82S16: −100μA
  S82S16: −250μA
- **Output follows complement of data input during Write (Non-blanked output)**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

F,N PACKAGE*



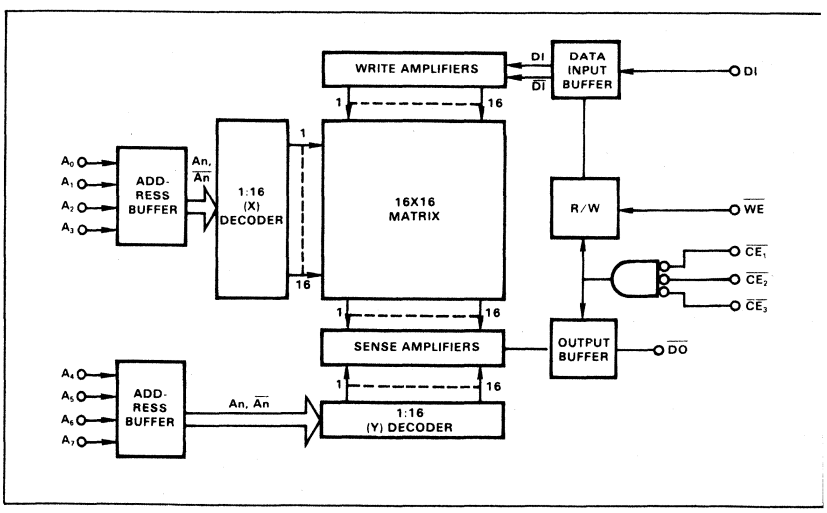
*F = Cerdip R = Flat Pak
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$
				82S16
Read	0	1	X	Stored $\overline{data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Diasabled	1	X	X	High-Z

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage	+5.5	Vdc
V_O	Off-state		
	Temperature range		°C
T_A	Operating		
	N82S16	0 to +75	
	S82S16	-55 to + 125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S16: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S16: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S16			S82S16			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage[1]								V
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[2]	V_{CC} = Min, I_{IN} = -12mA			-1.5			-1.5	
	Output voltage[1]	V_{CC}= Min							V
V_{OH}	High[3]	I_{OH} = -3.2mA	2.6			2.4			
V_{OL}	Low[4]	I_{OL} = 16mA			0.45			0.5	
	Input current[2]	V_{CC} = Max							μA
I_{IH}	High	V_{IN} = 5.5V			25			25	
I_{IL}	Low	V_{IN} = 0.45V			-100			-250	
	Output current								
$I_{O(OFF)}$	Hi-Z state[5]	$\overline{CE}_{1,2,3}$ = High, V_{OUT} = 5.5V			40			50	μA
		$\overline{CE}_{1,2,3}$ = High, V_{OUT} = 0.45V			-40			-50	
I_{OS}	Short-circuit[3,6]	$\overline{CE}$ = 1,2,3 = Low, V_{CC} = Max, V_O = OV	-20		-70	-20		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max			115			120	mA
	Capacitance	$\overline{CE}_{1,2,3}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

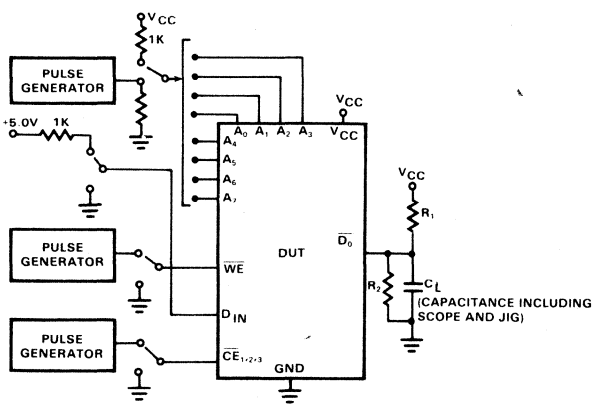
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S16: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S16: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S16			S82S16			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Access time									ns
T_{AA}	Address					50			70	
T_{CE}	Chip enable					40			40	
T_{CD}	Disable time	Output	Chip enable			40			40	ns
T_{WD}	Valid time	Output	Write enable			40			55	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	20			20			
T_{WHA}	Hold time			5			20			
T_{WSD}	Setup time	Write enable	Data in	40			50			
T_{WHD}	Hold time			5			10			
T_{WSC}	Setup time	Write enable	$\overline{CE}$	10			10			
T_{WHC}	Hold time			5			10			
	Pulse width									ns
T_{WP}	Write enable[8]			30			40			

NOTES
1. All voltage values are with respect to network ground terminal.
2. Test each input one at the time.
3. Measured with a logic low stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
4. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Duration of the short-circuit should not exceed 1 second.
7. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
8. Minimum required to guarantee a Write into the slowest bit.

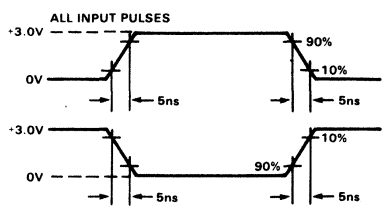
TEST LOAD CIRCUIT

LOADING CONDITION



VOLTAGE WAVEFORM

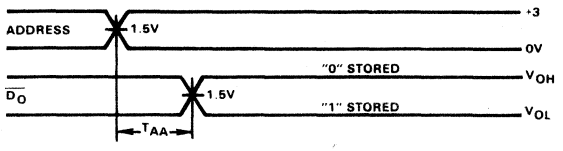
INPUT PULSES



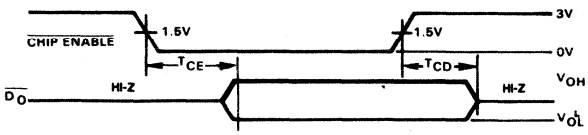
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE

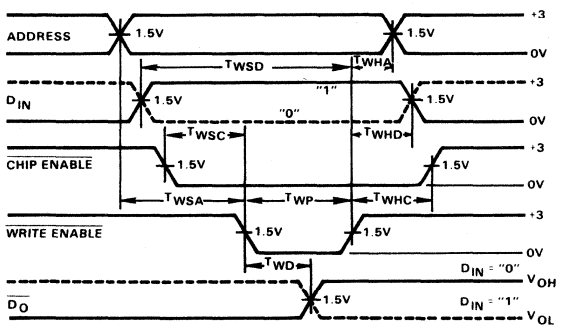


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/19 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

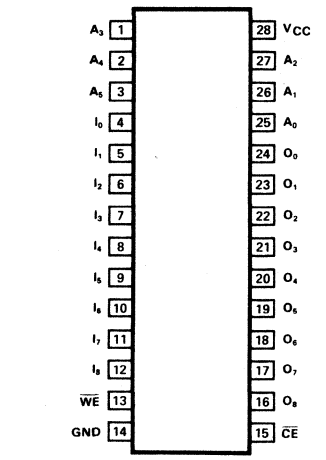
The 82S09/19 is available in the commercial and military temperature ranges. For the commercial temperature ranges (0°C to +75°C) specify N82S09/19, F or N and for the military temperature range (−55°C to +125°C) specify S82S09/19 I, R or F.

APPLICATIONS

- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

PIN CONFIGURATION

R,F,I,N PACKAGE*



F = Cerdip I = Ceramic
N = Plastic R = Flat Pak

FEATURES

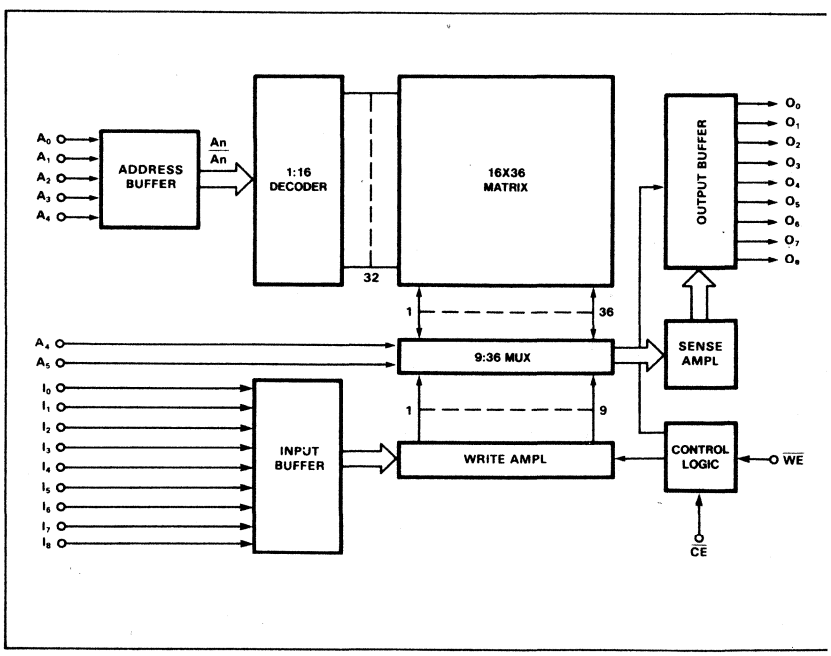
- **Address access time:**
  - **N82S09: 45ns max**
  - **S82S09: 80ns max**
  - **N82S19: 35ns max**
  - **S82S19: 55ns max**
- **Write cycle time:**
  - **N82S09/19: 45ns max**
  - **S82S09: 75ns max**
  - **S82S19: 55ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  - **N82S09/19: −100μA max**
  - **S82S09/19: −150μA max**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**
- **82S09 Output is Non-Blanked During Write**
- **82S19 Output is Blanked During Write**

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{O}_N$	
				82S09	82S19
Read	0	1	X	Complement of data stored	
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	1
Disabled	1	X	X	1	1

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
T_A	Temperature range		°C
	Operating		
	N82S09/19	0 to +75	
	S82S09/19	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[1,7]

N82S09/19: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S09/19: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER[1]		TEST CONDITIONS	N82S09/19			S82S09/19			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.2			
V_{IC}	Clamp[2]	V_{CC} = Min, I_{IN} = −12mA			−1.5			−1.5	
	Output voltage								V
V_{OL}	Low[3]	V_{CC} = Min, I_{OL} = 8.0mA			0.5			0.5	
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			25			40	
	Output current								μA
I_{OLK}	Leakage[4]	V_{CC} = Max, V_{OUT} = 5.5V			40			60	
I_{CC}	V_{CC} supply current[5]	V_{CC} = Max			190			200	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

Refer to notes on next page.

AC ELECTRICAL CHARACTERISTICS[7]

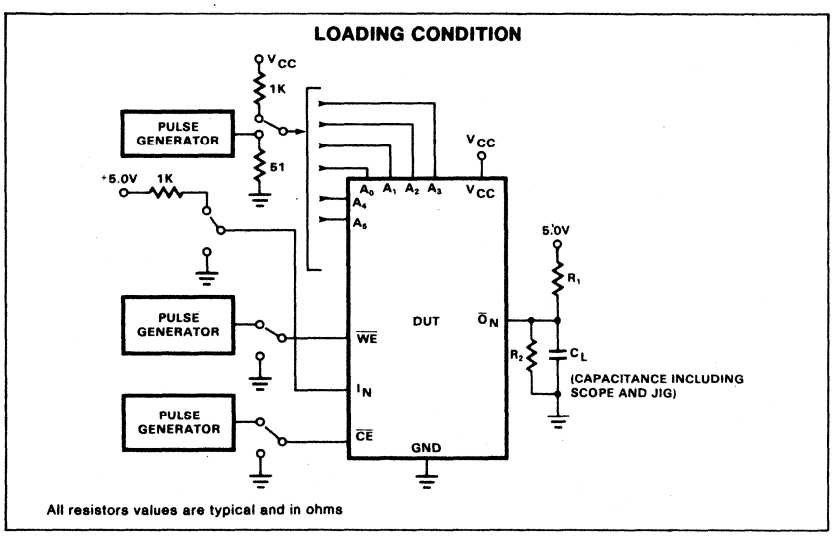
$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, for 82S09
$R_1 = 510\Omega$, $R_2 = 750\Omega$, $C_L = 30pF$, for 82S19
N82S19: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S19: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TO	FROM	N82S09			S82S09			N82S19			S82S19			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Access time															ns
T_{AA}	Address					45			80			35			60	
T_{CE}	Chip enable					30			50			25			40	
T_{CD}	Disable time	Output	Chip enable			30			50			25			35	ns
T_{WD}	Valid time	Output	Write enable			50			80			25			50	ns
T_{WR}	Write recovery time	Output	Write enable									25			50	
	Setup and hold time															ns
T_{WSA}	Setup time	Write enable	Address	5			10			5			10			
T_{WHA}	Hold time			5			20			5			10			
T_{WSD}	Setup time	Write enable	Data in	35			50			30			45			
T_{WHD}	Hold time			5			5			5			5			
T_{WSC}	Setup time	Write enable	$\overline{CE}$	5			10			5			10			
T_{WHC}	Hold time			5			10			5			10			
	Pulse width															ns
T_{WP}	Write enable[6]			35			50			35			50			

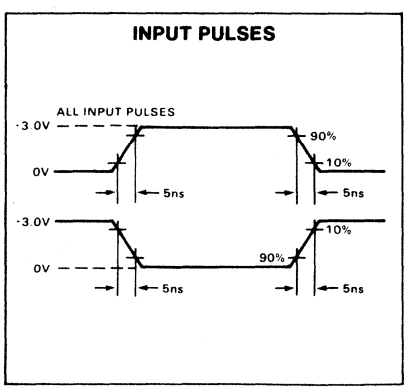
NOTES

1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT

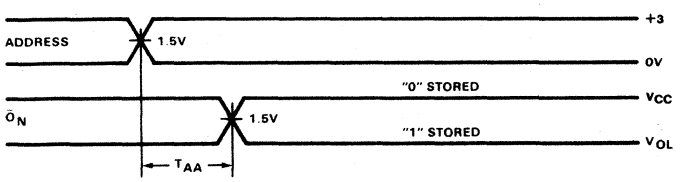


VOLTAGE WAVEFORM

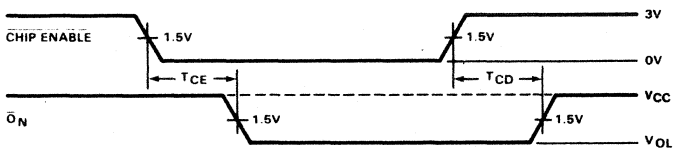


TIMING DIAGRAMS

READ CYCLE

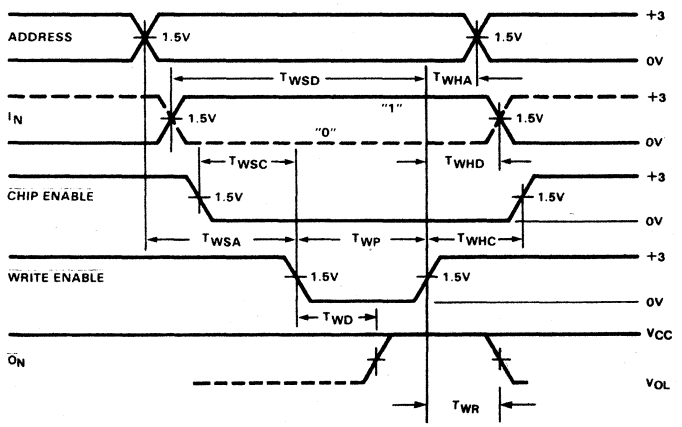


Address Access Time

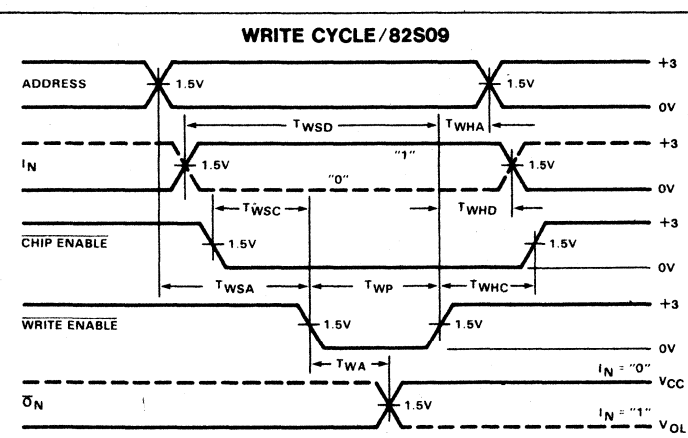


Chip Enable/Disable Times

WRITE CYCLE/82S19



WRITE CYCLE/82S09



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)
T_{WA}	Delay between beginning of Write Enable pulse and when data output reflects complement of data input.

OBJECTIVE SPECIFICATION 100422-F,N

DESCRIPTION

The 100422 device is a 256 word by 4 bit fully encoded ELC Read/Write random access memory designed for high speed scratch pad, control, and buffer storage applications. The 100422 contains voltage and temperature compensation circuits making it 100K family compatible. The 100422 with 15ns access time is available in a slim line 24 pin dual-in-line package. This circuit may be reconfigured as 512X2 or 1024X1 organization by utilizing the block select feature. Each block has its own, low active, Block Select to enable the output. Write enable, low active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data Outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply voltage. The input pull-down resistor to V_{EE} is 50,000 ohms typical for the Block Selects.

FEATURES

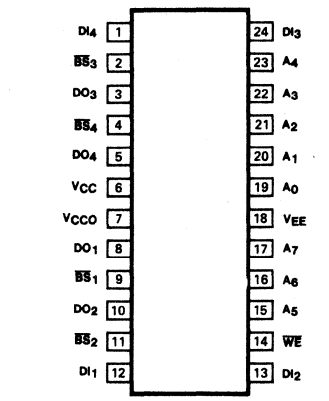
- **256 words X 4 bits organization**
- **Fully compatible with 100K series ECL families**
- **Address access time: 15ns (max)**
- **Low power dissipation of 0.8 mW/bit**
- **Operating temperature: 0°C to +75°C (ambient)**
- **Block select allows variable organization**

APPLICATIONS

- **High speed scratchpad**
- **Control and buffer storage**

PIN CONFIGURATION

F, N PACKAGE*



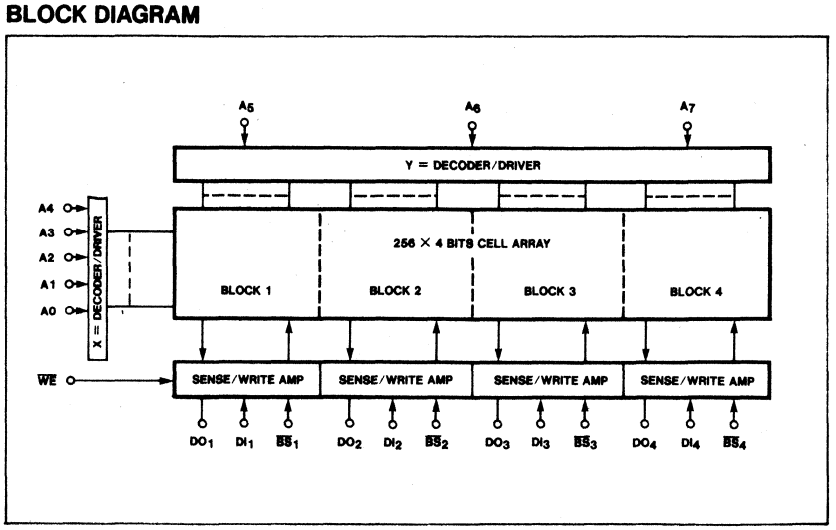
*F = Cerdip
N = Plastic

TRUTH TABLE (Positive Logic)

INPUT $\overline{BS}_N$	INPUT $\overline{WE}$	INPUT DI_N	OUTPUT DO_N	MODE
H	X	X	L	Disable
L	L	L	L	Write "O"
L	L	H	L	Write "1"
L	H	X	DO	Read

NOTES
H = High voltage level
L = Low voltage level
X = Don't care
N = Block 1-4

BLOCK DIAGRAM



OBJECTIVE SPECIFICATION 100422-F,N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	−8	Vdc
V_{IN}	Input voltage	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	temperature range		°C
T_A	Operating	0°C to +75	
T_J	Operating junction	125	
TS_{TG}	Storage	−55 to +125	

DC ELECTRICAL CHARACTERISTICS V_{CC} = OV, V_{EE} = −4.5V, RL = 50Ω to −2V, T_{AA} = 0°C to +75°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IL}	Low		−1.810			
V_{IH}	High				−.880	
V_{ILA}	Threshold				−1.475	
V_{IHA}	Threshold		−1.165			
	Output voltage					
V_{OL}	Low	V_{IL} = min	−1.810		−1.620	
V_{OH}	High	V_{IH} = max	−1.025		−.880	
V_{OLA}	Threshold	V_{IL} = max			−1.610	
V_{OHA}	Threshold	V_{IH} = min	−1.035			
I_{IL}	Low	V_{IL} = min			−6	mA
I_{IL}	$\overline{BS}$				10	
I_{IH}	High	V_{IH} = max			220	
I_{EE}	Supply current				220	
	Capacitance					pF
C_{IN}	Input				8	
C_{OUT}	Output				8	

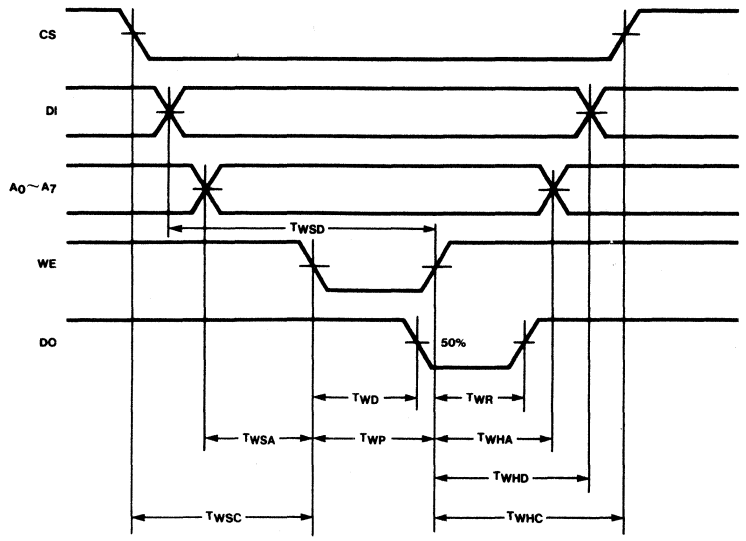
AC ELECTRICAL CHARACTERISTICS V_{CC} = OV, V_{EE} = 4.5, RI = 50Ω to −2V, TA = 0°C to +75°C

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_{CE}	Block select access time			4.5	ns
T_{CD}	Block select recovery time			4.5	ns
T_{AA}	Address access time			15.0	ns
T_{WP}	Write pulse width	8.0			ns
T_{WSA}	Address set up time[1]	3.0			ns
T_{WSC}	Block select set up time[1]	3.0			ns
T_{WSD}	Data set up time[1]	11.0			ns
T_{WHA}	Address hold time[1]	4.0			ns
T_{WHC}	Block select hold time[1]	4.0			ns
T_{WHD}	Data hold time[1]	4.0			ns
T_{WD}	Write disable time[1]			5.0	ns
T_{WR}	Write recovery time[1]			9.0	ns
t_r	Output rise time[2]				ns
t_f	Output fall time[2]				ns

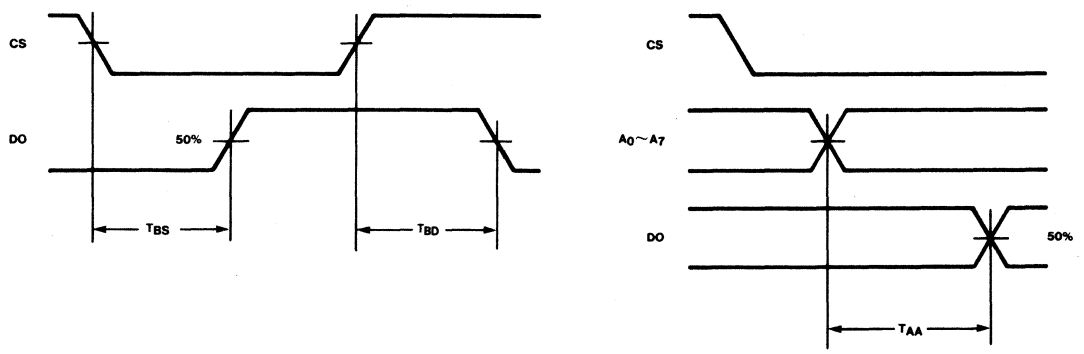
NOTES
1. TWP = 8.0ns
2. Measured between 10% and 90% points

TIMING DIAGRAMS

WRITE MODE



READ MODE



OBJECTIVE SPECIFICATION 10415-F

DESCRIPTION

The 10415 device is a 1024 word by 1 bit, fully decoded ECL Read Write Random Access Memory, designed for high speed scratch pad, control and buffer storage applications. The device also includes full address decoding on chip separate data in and non-inverting data out lines, an active low chip select and a 20ns maximum address access time (15ns max for 10415A).

FEATURES

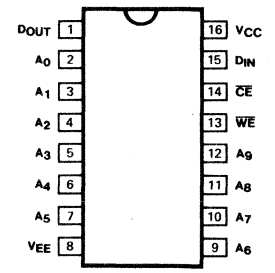
- **Organization: 1024 words of 1 bit.**
- **Fully compatible with 10K ECL families.**
- **Operating temperature: 0°C to 75°C.**
- **Address access time:**
  10415: 20ns max
  10415A: 15ns max
- **Low power dissipation: 7 mW/bit typical.**
- **Blanked outputs.**

APPLICATIONS

- **Buffer memory**
- **Scratch pad memory**
- **Writeable microcode store**

PIN CONFIGURATION

F PACKAGE



*F = Cerdip

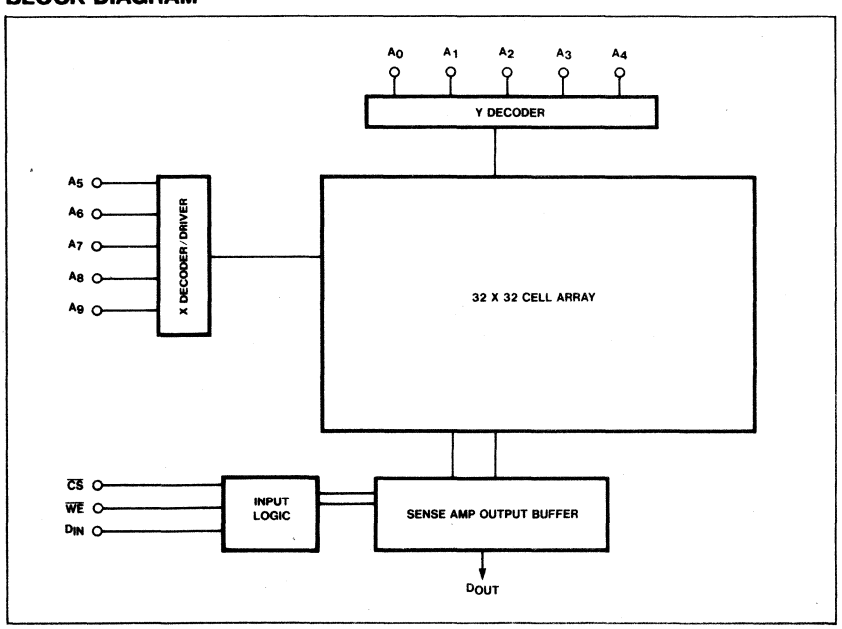
TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DI		
H	X	X	L	Disable
L	H	X	D_O	Read mode
L	L	H	L	Write mode Write 1
L	L	L	L	Write 0

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	−7	Vdc
V_O	Output voltage	+.5 to V_{EE}	Vdc
I_O	Output current	30	mA
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−55 to +150	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{EE} = −5.2V, Output load 50Ω to −2V

PARAMETER		TEST CONDITION	0°C		+25°C		+75°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Input voltage								
V_{IH}	High			− .840		− .810		− .720	V
V_{IL}	Low		−1.870		−1.850		−1.830		
V_{IHA}	Threshold		−1.145		−1.105		−1.045		
V_{ILA}	Threshold			−1.490		−1.475		−1.450	
	Output voltage								
V_{OH}	High	V_{IH} MAX	−1.0	− .840	− .960	− .810	− .900	− .720	V
V_{OL}	Low	V_{IL} MIN	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	
V_{OHA}	Threshold High	V_{IHA}	−1.020		− .980		− .900		
VOLA	Threshold Low	V_{ILA}		−1.645		−1.630		−1.605	
	Input current								
I_{IH}	High	V_{IH} MAX		220		220		220	μA
I_{IL}	Low	V_{IL} MIN			−6				
I_{IL}	Low	$\overline{CE}$			10				
I_{EE}	Supply Current	V_{IL} MIN				190			mA
	Capacitance								
C_{IN}						5			pF
C_{OUT}						5			

AC ELECTRICAL CHARACTERISTICS V_{EE} = −5.2V ± 5%

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
	Access time						ns
T_{AA}	Address[2] (10415)	Output	Address			20	
	(10415A)	Output	Address			15	
T_{CE}	Chip enable	Output	Chip enable			5	
T_{CD}	Disable time	Output	Chip enable			5	
T_{WR}	Write recovery	Output	Write enable			10	ns
T_{WD}	Write disable					6	
	Set up and hold time						ns
T_{WSA}		Write enable	Address	2			
T_{WHA}				2			
T_{WSD}		Write enable	Data in	12			ns
T_{WHD}				2			
T_{WSC}		Write enable	$\overline{CE}$	2			ns
T_{WHC}				2			
	Pulse width[1]						ns
T_{WP}				10			
t_r	Output rise time			.5			ns
t_f	Output fall time			.5			

NOTES

1. To guarantee a write into the slowest bit.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

SWITCHING TIMES TEST CIRCUIT

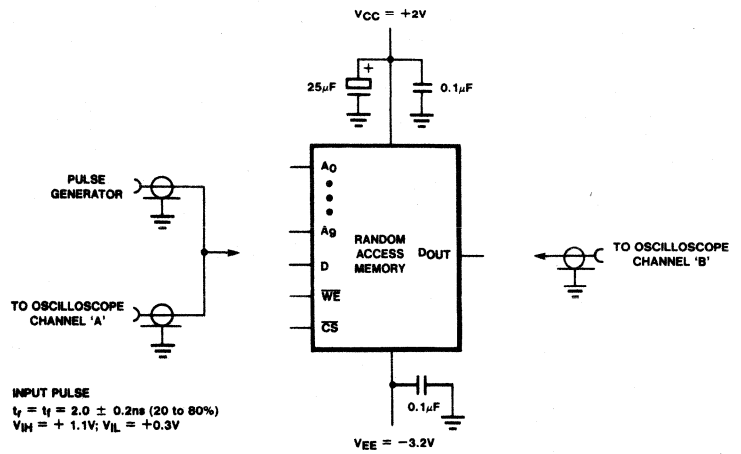
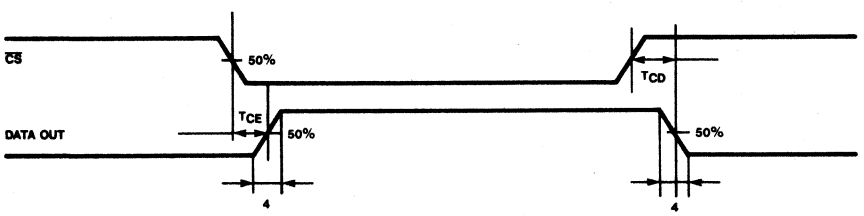
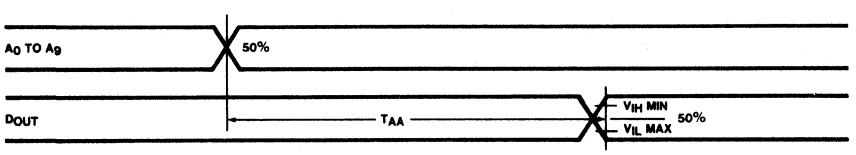


Figure 4

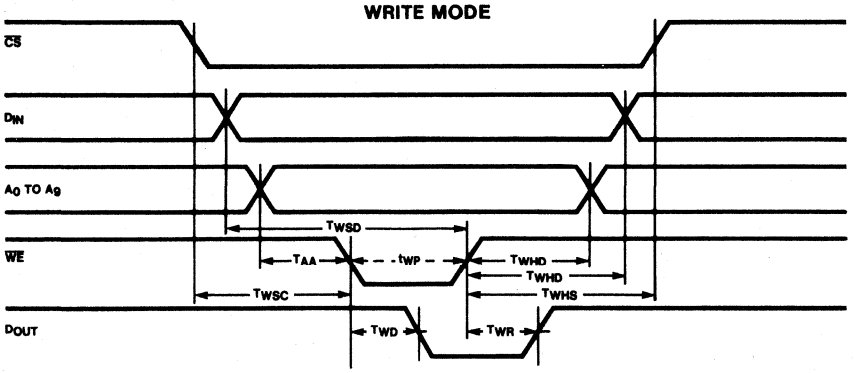
READ MODE PROPAGATION DELAY FROM CHIP SELECT



READ MODE PROPAGATION DELAY FROM ADDRESS



WRITE MODE



OBJECTIVE SPECIFICATION 100415-F

DESCRIPTION

The 100415 device is a 1024 word by 1 bit fully decoded ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. The 100415 contains voltage and temperature compensation circuits making it 100K family compatible. The device also includes full address decoding on chip, separate Data in and non-inverting Data out lines, an active low chip select input and a 20ns maximum address access time (15ns max for 100415A).

FEATURES

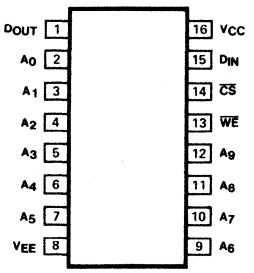
- **1024 words × 1 bit organization.**
- **Fully compatible with 100K series ECL families.**
- **Address access time:**
  100415: 20ns max
  100415A: 15ns max
- **Low power dissipation of 0.7mW/bit.**
- **Operating temperature: 0°C to 75°C (ambient).**
- **Blanked outputs.**
- **$\overline{CE}$ with 50K pulldown resistor.**

APPLICATIONS

- **Buffer memory.**
- **Scratch pad memory.**
- **Writeable microcode store.**

PIN CONFIGURATIONS

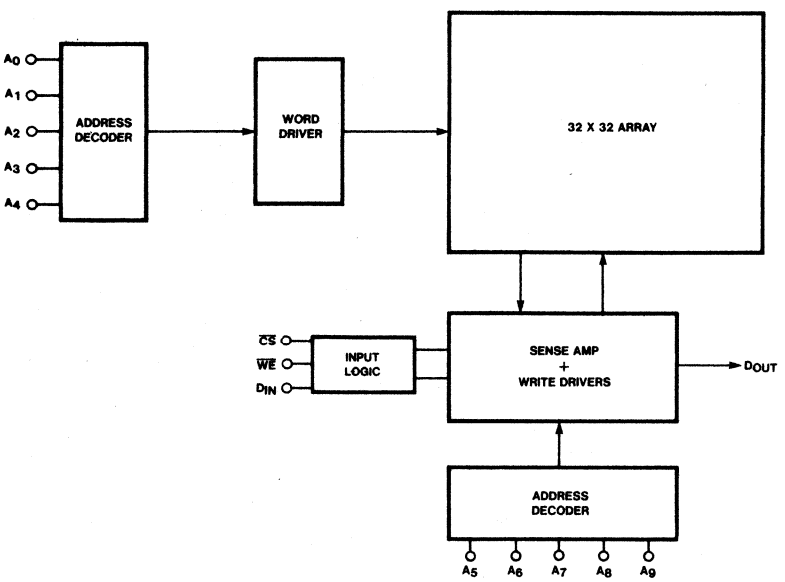
F PACKAGE



TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	D_{IN}	OUTPUT	MODE
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	−7	Vdc
V_{IH}	Input voltage	+.5V to V_{EE}	Vdc
V_{OH}	Output voltage	+.5V to V_{EE}	Vdc
I_O	Output source current	−30 to +0.1	mA
T_A	Operating	0 to +85	°C
T_J	Operating junction	125	°C
T_{STG}	Storage	−55 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{EE} −4.5V, V_{CC} = GND, $0 \leq T_A \leq 75°C$ Loading is 50Ω to −2.0V

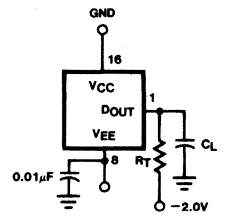
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		−1.810			
V_{IH}	High				−.880	
V_{ILA}	Threshold				−1.475	
V_{IHA}	Threshold		−1.165			
	Output voltage					V
V_{OL}	Low	V_{IL} = min	−1.810		−1.620	
V_{OH}	High	V_{IH} = max	−1.025		−.880	
V_{OLA}	Threshold	V_{IL} = max			−1.610	
V_{OHA}	Threshold	V_{IH} = min	−1.035			
I_{IL}	Low				6	mA
I_{IL}	$\overline{CE}$				10	
I_{IH}	High				220	
I_{EE}					180	mA

NOTES
1. To guarantee a write into the slowest bit.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Max at 25°C ambient.
4. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warm-up.

AC ELECTRICAL CHARACTERISTICS[5] V_{EE} = −4.5 ± 5%, 0°C ≤ T_A ≤ 75°C, V_{CC} = GND, Output load = 50Ω and 30pF to −2.0V.

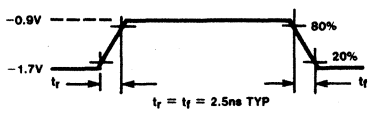
PARAMETER		TO	FROM	LIMIT		UNIT
				Min	Max	
	Access time					ns
T_{AA}	Address[2, 3] 100415	Output	Address		20	
	100415A	Output	Address		15	
T_{CE}	Chip enable	Output	Enable		5	
T_{CD}	Chip disable	Output	Disable		5	
	Pulse width					ns
T_{WP}	Write enable[1]			10		
	Set up and hold times					ns
T_{WSD}	Set up time	Write enable	Data in	12		
T_{WHD}	Hold time			2		
T_{WSA}	Set up time	Write enable	Address	2		ns
T_{WHA}	Hold time			2		
T_{WSC}	Set up time	Write enable	Chip select	2		
T_{WHL}	Hold time			2		
T_{WD}	Write disable	Output	Write enable		6	ns
T_{WR}	Write recovery time				10	
t_r	Output rise time			.5	5 (TYP)	ns
t_f	Output fall time			.5	5 (TYP)	
	Capacitance					pF
C_{IN}	Input				5	
C_{OUT}	Output				5	

LOADING CONDITIONS



NOTE
C_L = 30pF including jig and stray capacitance
R_T = 50Ω termination of scope

INPUT LEVELS



All timing measurements referenced to 50% of input levels

READ MODE PROPAGATION DELAY FROM CHIP SELECT

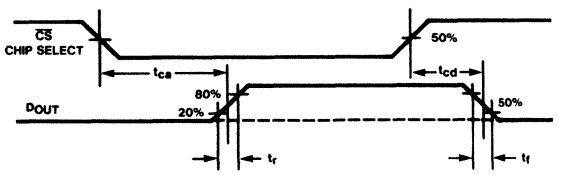


Figure 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

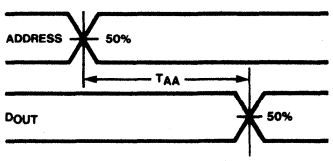
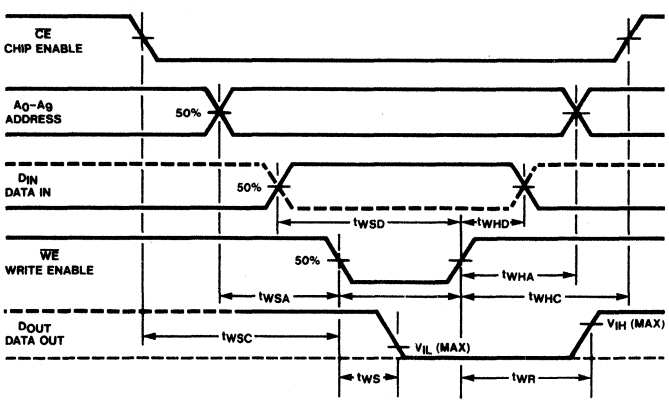


Figure 1b

WRITE MODE



NOTE
Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Figure 2

DESCRIPTION

The 82S210 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

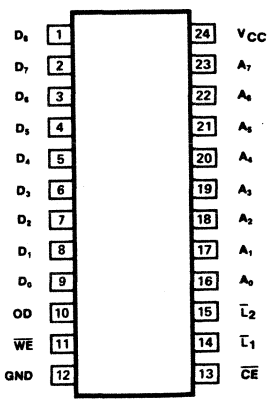
$\overline{WE}$ causes the present address state to be held in the address latches, independent of any other control signals. A positive pulse on both $\overline{L}$ lines will cause a new address state to be strobed into the latches.

FEATURES

- **Access time:**
  Address: 60ns max
  Strobe: 70ns max
- **On-chip address latches**
- **Tri-state outputs**
- **Schottky clamped TTL**
- **9th Bit for Parity or Tag**

PIN CONFIGURATION

82S210
F, N PACKAGE*



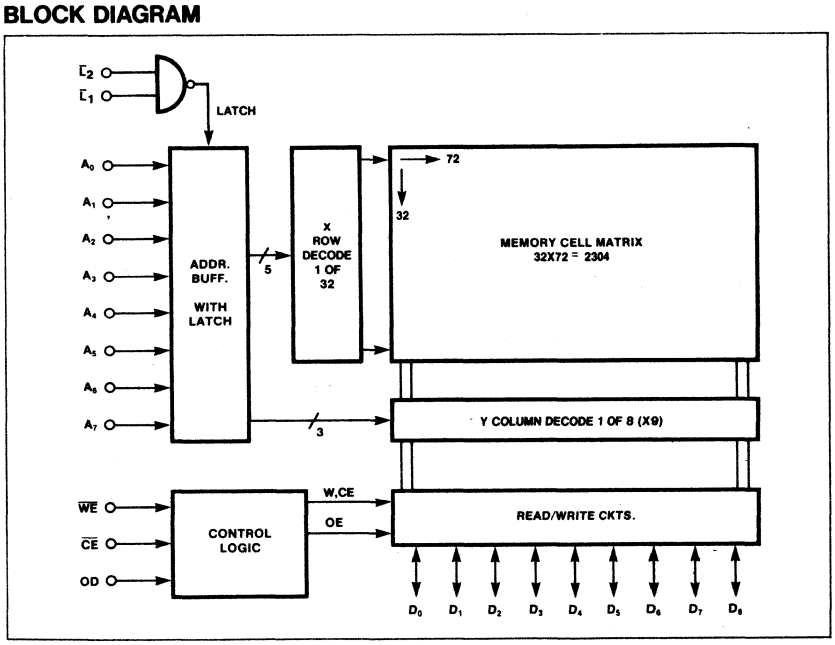
*F = Cerdip N = Plastic

TRUTH TABLE

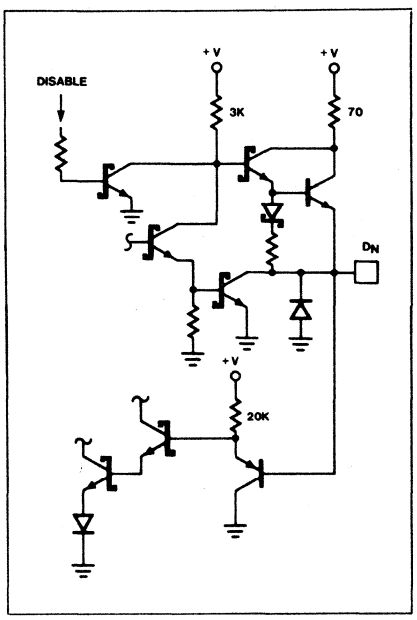
MODE	$\overline{WE}$	$\overline{CE}$	OD	$\overline{L}_1$	$\overline{L}_2$	D_N IN/OUT
Disable output	X	X	1	X	X	High Z
Disable R/W	X	1	X	X	X	High Z
Write	0	0	1	X	X	Data in
Read	1	0	0	X	X	Data out
Transparent address	X	X	X	1	1	—
Hold address	X	X	X	0	X	—
Hold address	X	X	X	X	0	—

X = Don't care

BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[2]					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp[3]	$I_{IN} = -12mA$			−1.2	
	Output voltage[2]	$\overline{CE}$, OD = Low, $\overline{WE}$ = High				V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
	Input current					μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100	
I_{IH}	High	V_{IN} +5.5V			25	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
		CE = High, $V_{OUT} = 0.5V$			−100	
I_{OS}	Short circuit[3,4]	$\overline{CE}$ = OD = Low, $\overline{WE}$ = High, V_{OUT} = 0V, Stored High	−20		−70	mA
I_{CC}	Supply current				185	mA
	Capacitance	$\overline{CE}$ = High or OD = High				pF
C_{IN}	Input	$V_{CC} = 5.0V$				
C_{OUT}	Output	$V_{IN} = 2.0V$		5		
		$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
T_{AA}	Address access time	D_N	A_N			60	ns
T_{OE}	Output enable time	D_N	OD	5		35	ns
T_{CE}	Output enable time	D_N	$\overline{CE}$			35	
T_{OD}	Output disable time	D_N	OD			35	ns
T_{CD}	Output disable time	D_N	$\overline{CE}$			35	
T_{WP}	Write pulse width		$\overline{WE}$	40			ns
T_{SA}	Address setup time	$\overline{WE}$	A_N	10			ns
T_{HA}	Address hold time	A_N	$\overline{WE}$	10			
T_{SD}	Data setup time	$\overline{WE}$	D_N	35			ns
T_{HD}	Data hold time	D_N	$\overline{WE}$	10			
T_{SC}	Chip enable setup time	$\overline{WE}$	$\overline{CE}$	5			ns
T_{HC}	Chip enable hold time	$\overline{CE}$	$\overline{WE}$	5			
T_{SO}	OD setup time	$\overline{CE}$	OD	5			ns
T_{HO}	OD hold time	OD	$\overline{CE}$	5			
(To guarantee High Z state during entire write cycle)							

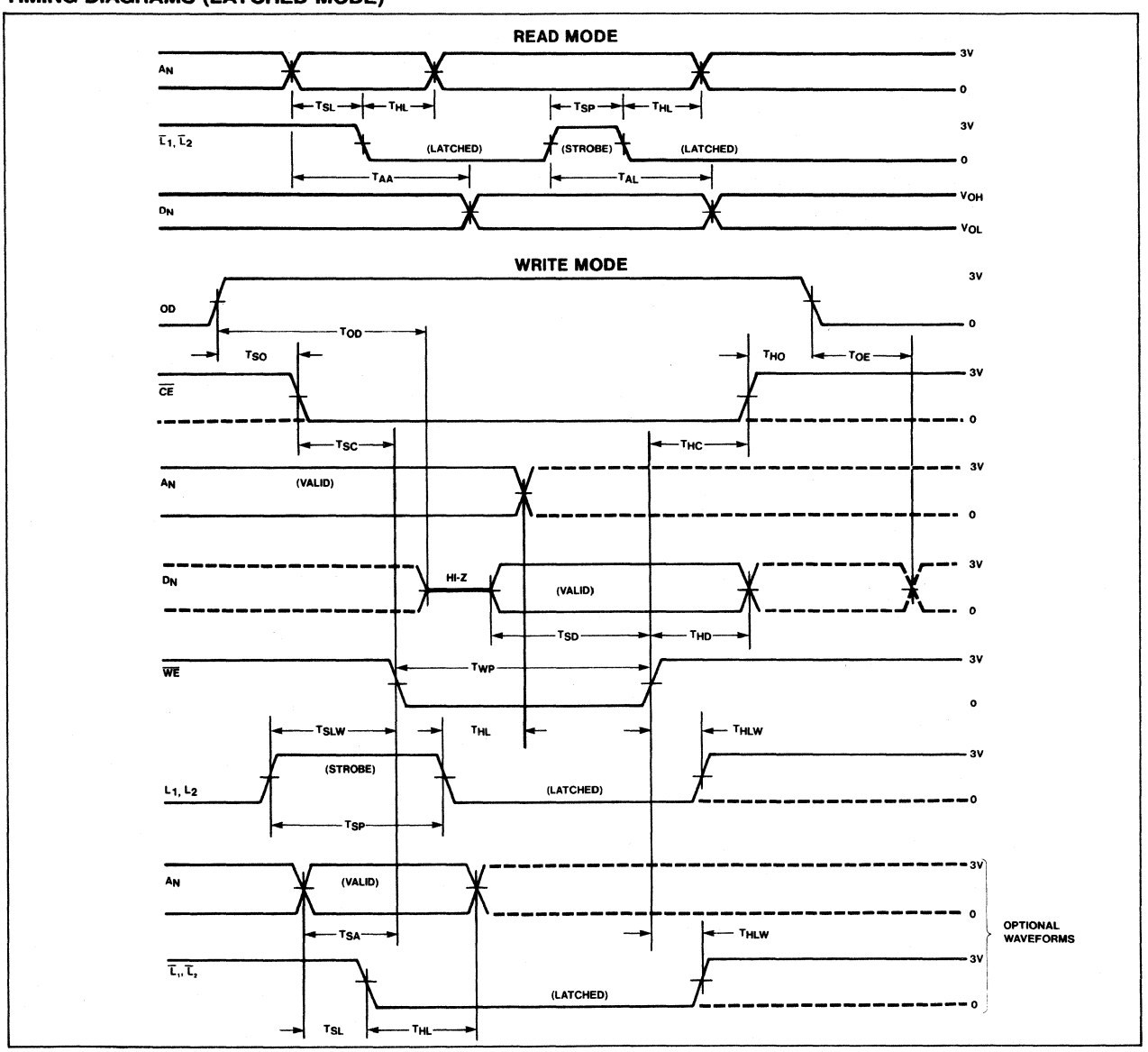
NOTES

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. Measured on one pin at a time.
4. Duration of test should not exceed one second.

AC CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$ (Continued)

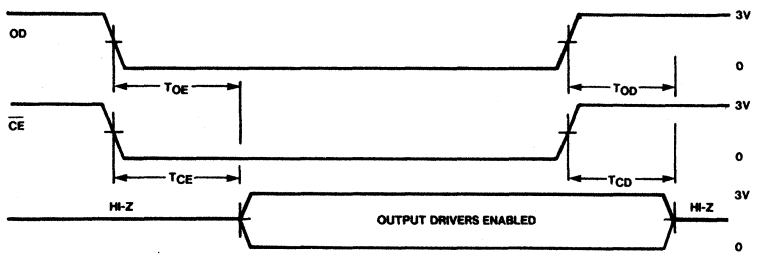
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
T_{SP}	Strobe pulse width		$\overline{L}$	20			ns
T_{SL}	Latch setup time	$\overline{L}$	A_N	5			ns
T_{HL}	Latch hold time	A_N	$\overline{L}$	10			
T_{SLW}	Strobe setup time	$\overline{WE}$	$\overline{L}$	15			ns
T_{HLW}	Latch hold after write	$\overline{L}$	$\overline{WE}$	10			
T_{AL}	Strobe access time	D_N	$\overline{L}$			70	ns

TIMING DIAGRAMS (LATCHED MODE)

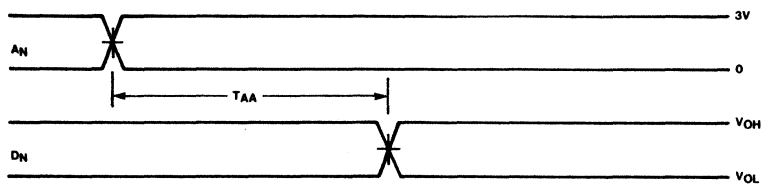


TIMING DIAGRAMS (TRANSPARENT MODE $\overline{L1} = \overline{L2} = 1$)

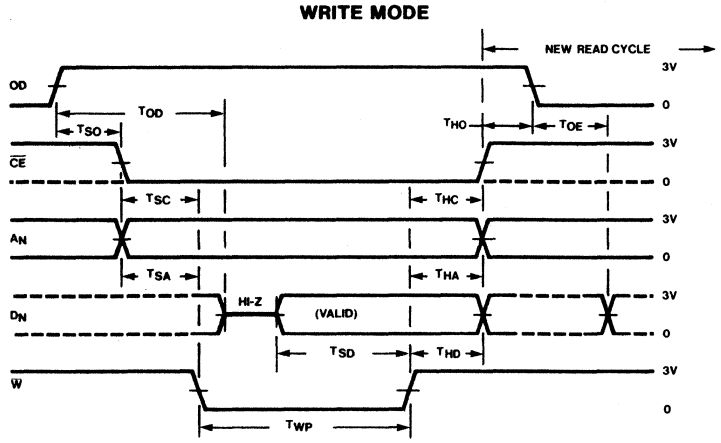
ENABLE / DISABLE



READ MODE



WRITE MODE



CAUTION = Data Bus conflict can occur with $\overline{CE} = 0$. Apply Data source after T_{OD} (max.) and remove Data Source before T_{OE} (min.).

OBJECTIVE SPECIFICATION 82S212-F

DESCRIPTION

The organization of this device allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, pushdown stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S212 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

FEATURES

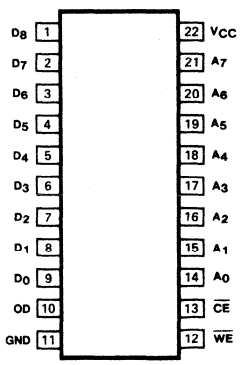
- Address access time: 45ns max
- Power dissipation: 0.3 mW/bit
- Tri-state outputs
- Schottky clamped TTL

APPLICATIONS

- Cache memory
- Buffer storage
- Writable control store

PIN CONFIGURATION

F PACKAGE*



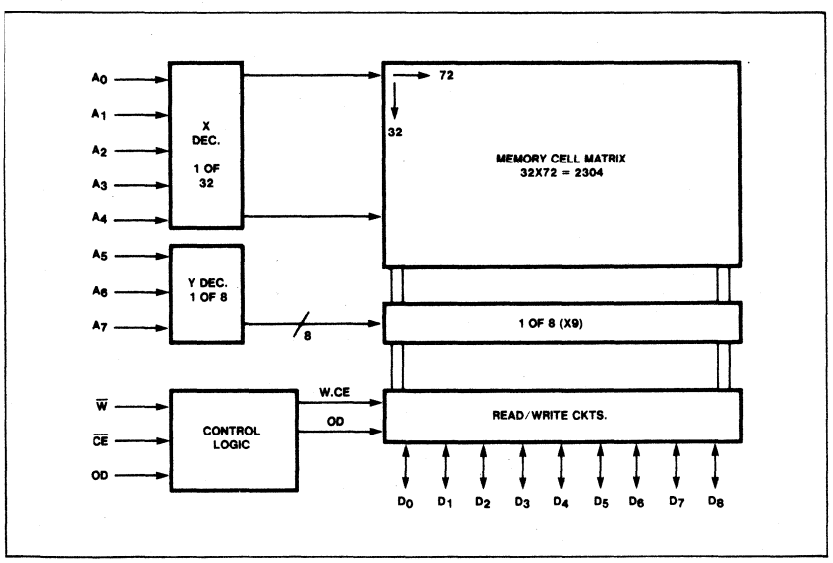
*F = Cerdip

TRUTH TABLE

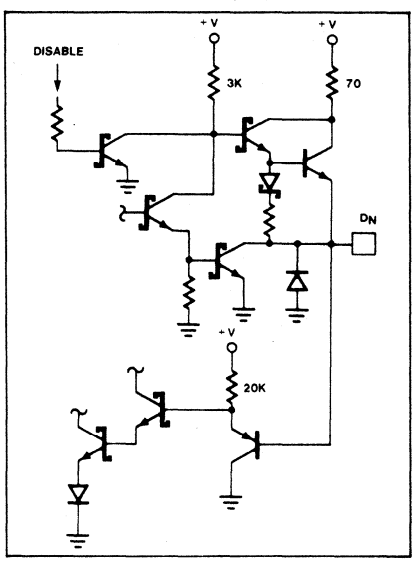
MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	High Z
Disable R/W	X	1	X	High Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS[2]			UNIT
			Min	Typ[3]	Max	
	Input voltage[2]					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp[4]	$I_{IN} = -12mA$		−0.8	−1.2	
	Output voltage[2]					V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4	3.3		
	Input current					μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100	
I_{IH}	High	$V_{IN} = 5.5V$			25	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High or OD = High, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High or OD = High, $V_{OUT} = 0.5V$			−100	
I_{OS}	Short circuit[4, 5]	$\overline{CE}$ = OD = Low, $V_{OUT} = 0V$	−20		−70	mA
I_{CC}	Supply current			135	185	mA
	Capacitance	$V_{OUT} = 2.0V$, $\overline{CE}$ = High or OD = High				pF
C_{IN}	Input	$V_{CC} = 5.0V$		5		
C_{OUT}	Output	$V_{IN} = 2.0V$		8		

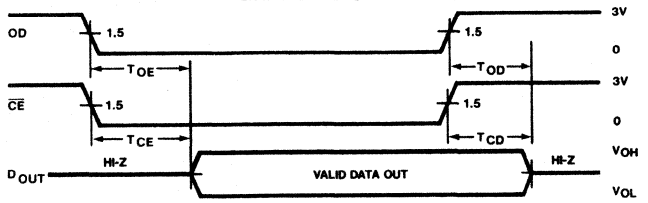
AC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
	Access time						ns
T_{AA}	Address	Output	Address			45	
	Enable time						ns
T_{OE}	Output	Output	OD	5		25	
T_{CE}	Output	Output	Chip enable			25	
	Disable time						ns
T_{OD}	Output	Output	OD			25	
T_{CD}	Output	Output	Chip enable			25	
	Pulse width						ns
T_{WP}	Write			25			
T_{WSC}	Setup time	Write	Chip enable	5			
T_{WHD}	Hold time	Chip enable	Write	5			
T_{WSD}	Setup time	Write	Data	25			
T_{WHD}	Hold time	Data	Write	5			
T_{WSA}	Setup time	Write	Address	5			
T_{WHA}	Hold time	Address	Write	5			
T_{SO}	Setup time (from disabled state)	Chip enable	OD	5			
T_{HO}	Hold time	OD	Chip enable	5			

NOTES
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.

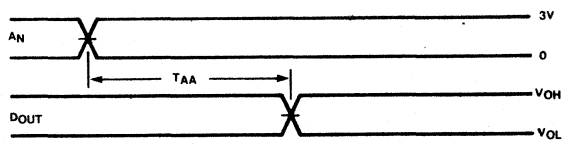
TIMING DIAGRAMS

ENABLE/DISABLE

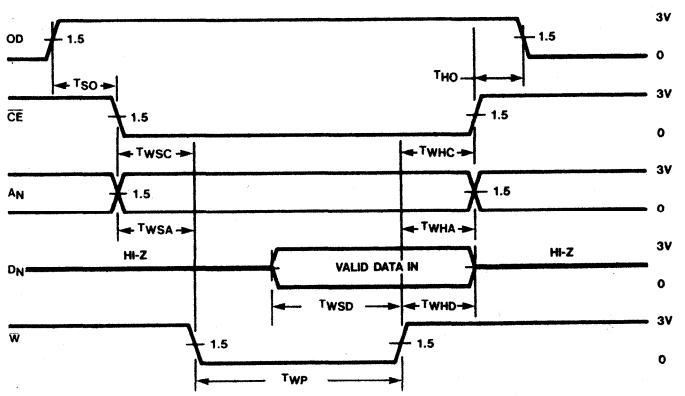


NOTE
Assumes T_{AA} from address to valid data $\overline{W}$ = high

READ MODE



WRITE MODE



CAUTION = Data Bus conflict can occur with $\overline{CE}$ = 0, apply data source after T_{OD} (max.) and remove data source before T_{OE} (min.).

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X300 based system. Internal circuitry is provided for direct use in 8X300 applications. When used with the 8X300, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-state outputs.

The 8X350 is available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N8X350-F, and for the military temperature range (−55°C to +125°C) specify S8X350-F.

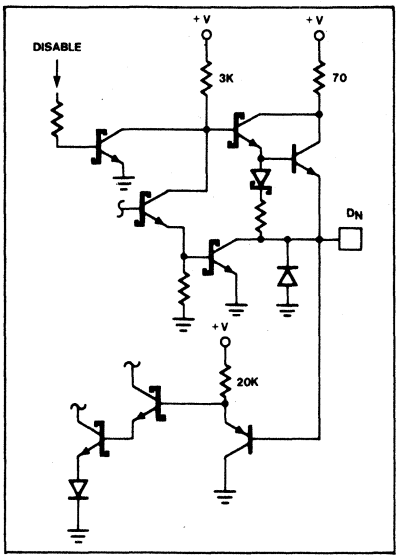
FEATURES

- **On-chip address latches**
- **3-state outputs**
- **Schottky clamped TTL**
- **Internal control logic for 8X300 system**
- **Directly interfaces with the 8X300 bipolar microprocessor with no external logic**
- **May be used on left or right bank**

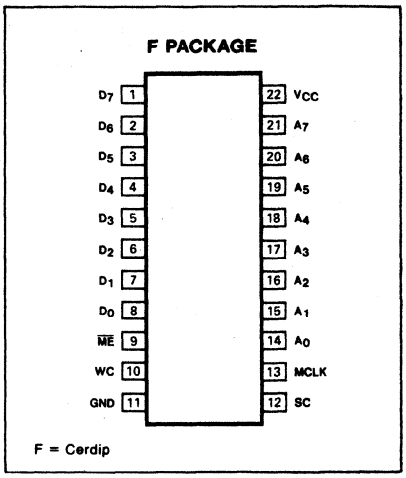
APPLICATIONS

- **8X300 working storage**

TYPICAL I/O STRUCTURE



PIN CONFIGURATION



F = Cerdip

ABSOLUTE MAXIMUM RATINGS

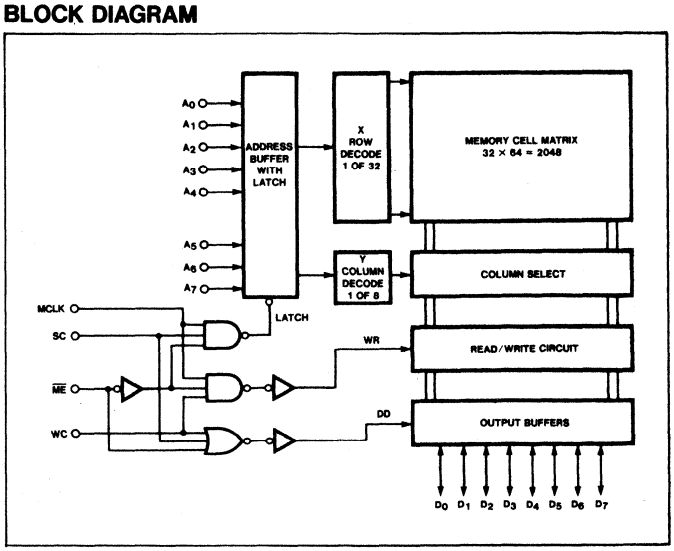
	PARAMETER[1]	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N8X350	0 to +75	
	S8X350	−55 to +125	
T_{STG}	Storage	−65 to +150	

TRUTH TABLE

Note X = Don't care

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address Disable data out	1	X	X	X	High Z
Input new address	0	1	0	1	Address High Z
Hold address Disable data out	0	1	0	0	High Z
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	High Z
Hold address Read data	0	0	0	X	Data out
Undefined state[12]	0	1	1	1	—
Hold address[12] Disable data out	0	1	1	0	High Z

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS[2]

N8X350: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S8X350: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	N8X350			S8X350			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = −12mA			−1.2			−1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA			0.5			.5	
V_{OH}	High[1,5]	I_{OH} = −2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								μA
$I_{O(OFF)}$	High Z state	$\overline{ME}$ = High, V_{OUT} = 5.5 V			40			60	μA
		$\overline{ME}$ = High, V_{OUT} = 0.5 V			−100			−100	
I_{OS}	Short circuit[3,6]	SC = WC, $\overline{ME}$ = Low, V_{OUT} = 0V, Stored High	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max			185			185	mA
	Capacitance	$\overline{ME}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS[2,9]

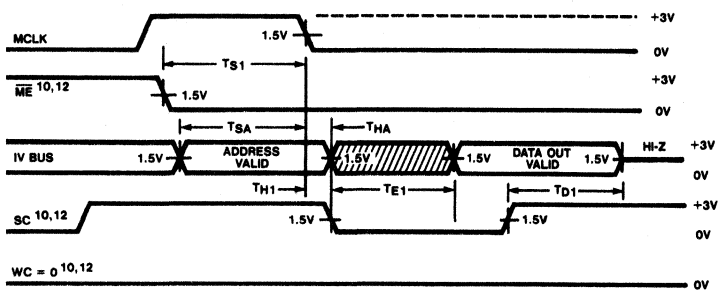
N8X350: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S8X350: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

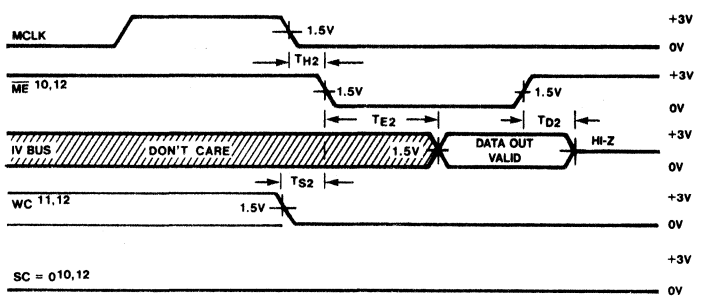
PARAMETER		TO	FROM	N8X350			S8X350			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Enable time									ns
T_{E1}	Output	Data out	SC−			35			40	
T_{E2}	Output	Data out	$\overline{ME}$−			35			40	
	Disable time									ns
T_{D1}	Output	Data out	SC+			35			40	
T_{D2}	Output	Data out	$\overline{ME}$+			35			40	
	Pulse width									ns
T_W	Master clock[8]			40			50			
	Setup and hold time									ns
T_{SA}	Setup time	MCLK−	Address	30			40			
T_{HA}	Hold time	Address	MCLK−	5			10			
T_{SD}	Setup time	MCLK−	Data in	35			45			
T_{HD}	Hold time	Data in	MCLK−	5			10			
T_{S3}	Setup time	MCLK−	$\overline{ME}$−	40			50			
T_{H3}	Hold time	$\overline{ME}$+	MCLK−	5			5			
T_{S1}	Setup time	MCLK−	$\overline{ME}$−	30			40			
T_{H2}	Hold time	$\overline{ME}$−	MCLK−	5			5			
T_{S2}	Setup time	$\overline{ME}$−	SC−,WC−	0			5			
T_{H1}	Hold time	SC−	MCLK−	5			5			
T_{H4}	Hold time	WC−	MCLK−	5			5			

TIMING DIAGRAMS

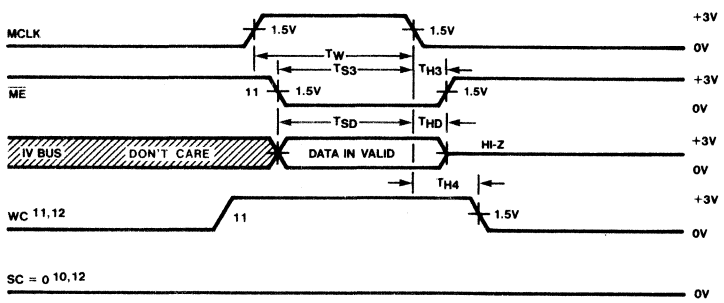
TRANSPARENT ADDRESS READ CYCLE



LATCHED ADDRESS READ CYCLE



LATCHED ADDRESS WRITE CYCLE



NOTES

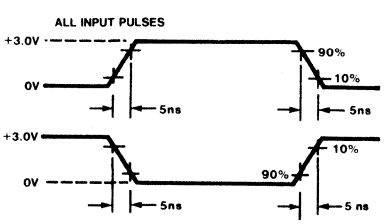
1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
   Typical thermal resistance values of the package at maximum temperature are:
   Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
   Θ_{JA} junction to ambient - still air - 90°C/watt
   Θ_{JA} junction to case - 20°C/watt
3. Test each pin one at a time.
4. Measured with a logic low stored Output sink current is supplied through a resistor to V_{CC}.
5. Measured with a logic high stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X300 based system with the data and address pins tied to the IV Bus.
10. SC + $\overline{ME}$ = 1 to avoid bus conflict.
11. WC + $\overline{ME}$ = 1 to avoid bus conflict.
12. The SC and WC outputs from the 8X300 are never at 1 simultaneously.

TIMING DEFINITIONS

T_{S1}	Required delay between beginning of Master Enable low and falling edge of Master Clock.
T_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
T_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
T_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes low.
T_{E1}	Delay between beginning of Select Command low and beginning of valid data output on the IV Bus.
T_{D1}	Delay between when select Command becomes high and end of valid data output on the IV Bus.
T_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes low.
T_{E2}	Delay between when Master Enable becomes low and beginning of valid data output on the IV Bus.
T_{D2}	Delay between when Master Enable becomes high and end of valid data output on the IV Bus.
T_{S2}	Required delay between when Select Command or Write Command becomes low and when Master Enable becomes low.
T_W	Minimum width of the Master Clock pulse.
T_{S3}	Required delay between when Master Enable becomes low and falling edge of Master Clock.
T_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes high.
T_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
T_{HD}	Required delay between falling edge of Master Clock and end of valid data input on the IV Bus.
T_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes low.

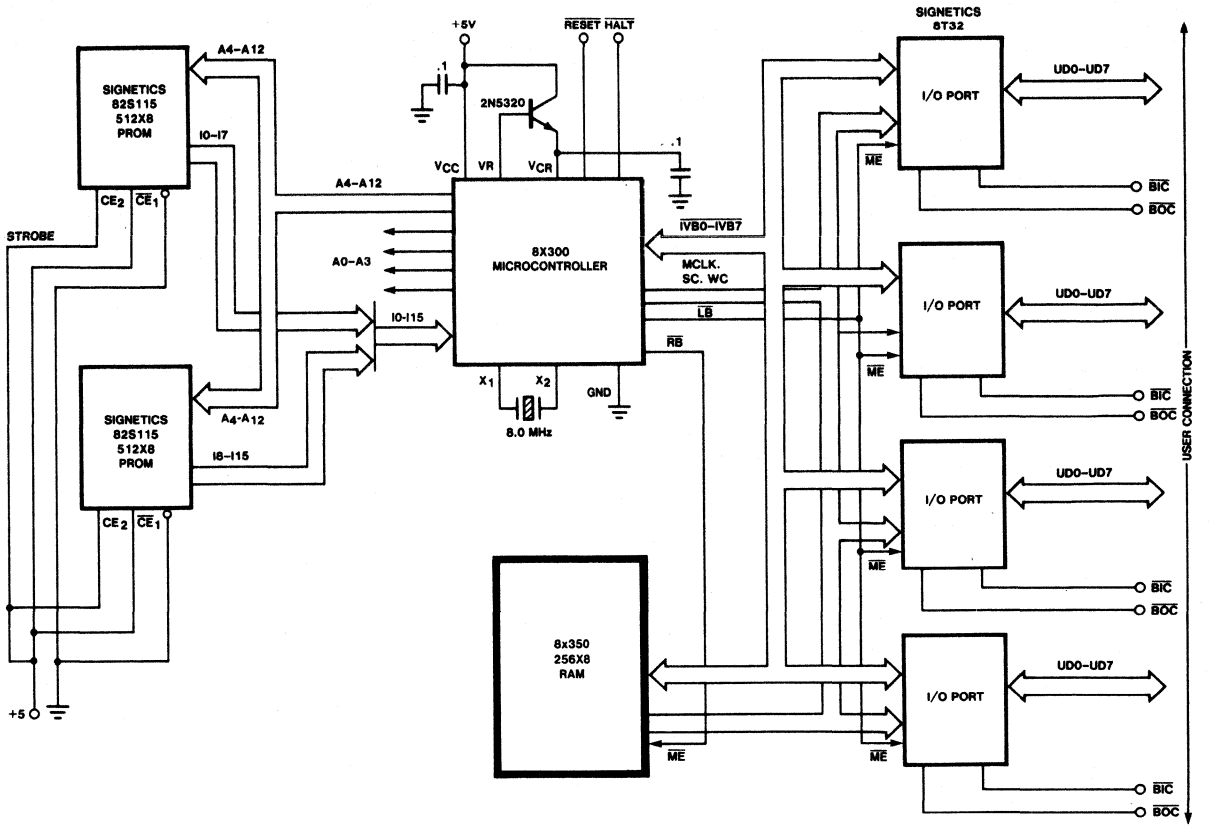
VOLTAGE WAVEFORM

INPUT PULSES



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

YPICAL 8X350 APPLICATION



PROGRAMMING

The Signetics family of Schottky PROMs are high performance bipolar devices which use a nickel/chromuim (nichrome) alloy fuse to provide the many benefits of field programming. All Signetics Schottky PROMs use a common fuse design and programming circuitry. This means that a programmer capable of programming any Signetics PROM should program the entire family. Because of the pinout variation a small selection of socket adapters may be required. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming (except the 82S115 which has two pins: FE_1 and FE_2). The programming voltages and timing requirements make unintentional programming virtually impossible. Arrays of devices may be programmed in the users circuit, if desirable, and isolation of programming voltages is provided.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers equipment is available on request from Bipolar Memory Marketing.

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Records of programming yield, by device type, should be kept and any downward trend or sudden change should be considered as an indication of a need to recalibrate programming equipment.

The following information is provided for reference and completeness of our data sheets.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT.

The generic family of Schottky PROMs uses no special pins for programming. The programming mode is evoked by raising the V_{CC} pin to +8.75 ± .25V. This voltage is referred to as V_{CCP}. The address pins remain TTL compatible and are used to address the unique word to be programmed. The outputs are used to supply fusing current in the programming mode.

Programming is performed one bit at a time, the word address is set up on the address inputs and the fuse to be programmed is selected by raising the output (corresponding to the bit in the word) to +17V ± 1V. This voltage is known as V_{OPF} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{OPF} power supply and circuitry. I_{OPF} is the current which should be drawn by the part during the programmming sequence. V_{OPF} should be maintained and I_{OPF} monitored. If the current is not within specification, reliable fusing can not be assured.

Unprogrammed parts are supplied with all bits "zero", only the bits intended to be "one" will be programmed.

A fuse which does not blow during the first programming cycle should be considered a defective device and should be discarded.

Verification of the device may be performed after all addresses have been programmed

PROGRAMMING[4]

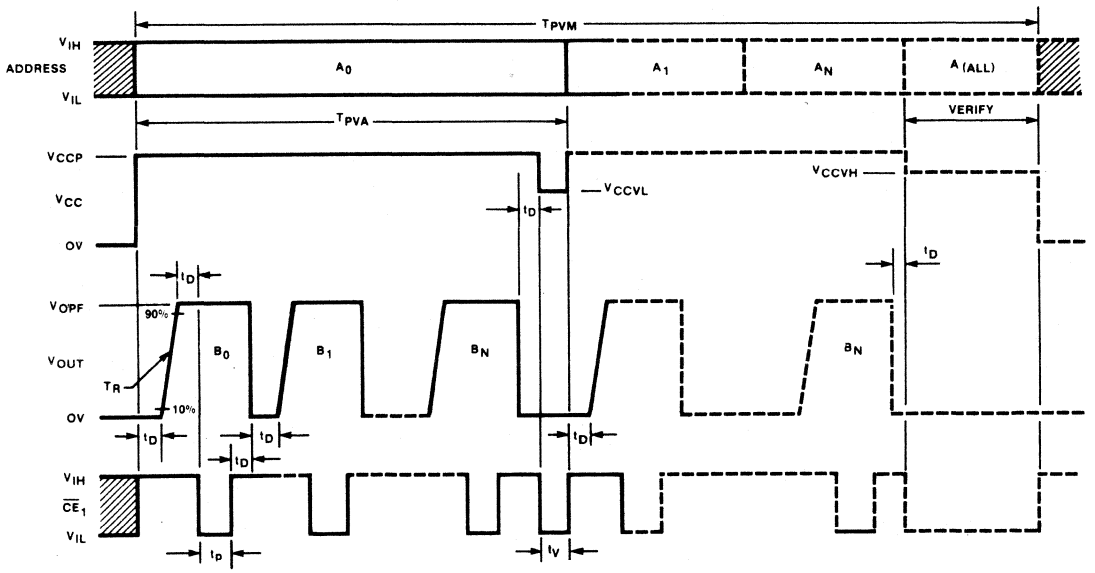
PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 + 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			−500	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_p	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
T_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment. Programming procedure for devices not listed in table 1 are found with the device data sheet.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC} (10K resistor is the pullup resistor for open collector devices).
2. Consult table 1 for CE conditions.
3. Select the Address to be programmed and raise V_{CC} to V_{CCP}.
4. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time. Note leading edge rise time restrictions.
5. After t_D delay, pulse the $\overline{CE}_X$ input to logic low for a time t_P.
6. After t_D delay, remove V_{OPF} from the programmed output.
7. Repeat steps 4 through 6 to program other bits at the same address.
8. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_X$ input. All programmed outputs should remain in the logic high state.
9. After t_D delay, repeat steps 3 through 8 to program and verify all other address locations.
10. After t_D delay, raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_X$, and cycling through all device addresses.

	$\overline{CE}$	$\overline{CE}_1$	$\overline{CE}_2$	CE_3	CE_4	$\overline{CE}_X$
82S23/123	H					$\overline{CE}$
82S126/129		H	L			$\overline{CE}_1$
82S130/131	H					$\overline{CE}$
82S141		L	H	H	H	$\overline{CE}_2$
82S147	H					$\overline{CE}$
82S137/137A		L	H			$\overline{CE}_2$
82S181		L	H	H	H	$\overline{CE}_2$
82SS181		L	H	H	H	$\overline{CE}_1$
82S183		L	H	H	H†	$\overline{CE}_2$
82S185/185A	H					$\overline{CE}$
82S191		H	H*	H		$\overline{CE}_1$
82S2708	H					$\overline{CE}$

NOTES
*CE_2 †CE_4 = strobe

Programming equipment for Signetics PROMs

Kontron
700 S. Claremont St.
San Mateo Ca 94402

Data I/O
P.O. Box 308
1297 N.W. Mall
Issaquah, WA 98027

Pro-Log Corp.
2411 Garden Rd.
Monterey, CA 93940

Stag Systems, Inc.
1120 San Antonio Rd.
Palo Alto, CA 94303

GENERIC RELIABILITY DATA FOR SIGNETICS PROMS

Periodically, failure rates are calculated for all current die process families based upon accelerated life test data accumulated during reliability engineering programs (primarily SURE II data). Because of widespread interest among PROM users about reliability—especially nichrome fuse reliability—Signetics has placed special emphasis on PROM testing. This report presents the latest (February, 1976) failure rate data on PROMs, based upon 100 million (25°C) device hours and 136 *billion* nichrome fuse (25°C) hours.

TTL PROM RELIABILITY TESTING HISTORY

Signetics performed reliability studies of fused and unfused nichrome links in 1971, subjecting unfused links to 5 times normal current and fused links to 12 volts. In late 1971, Field Programmable Read Only Memories (PROMs) employing the non-Schottky TTL multi-emitter fuse matrix design were offered for sale. Reliability tests were performed during 1971 to 1973 on "single notch" nichrome link product. A few program rejects were detected during the first measurement timepoint (168 hours) of operating life stress with no additional program rejects observed from 168 hours on out to 2000 hours. During that period, program yield (and probably product reliability) was found to be highly influenced by the programming procedure used.

During 1974, reliability tests were started on "second generation" TTL Schottky PROM Products. The "second generation" products use standard Schottky product processing with the addition of nichrome fuses. These products have a diode fusing matrix, use bar fuses, and are designed to supply increased current densities during fusing to enhance fuse reliability and increase programming yields. The reliability data to date is summarized in the table "PROM Life Test Summary: Std. Aluminum Schottky DLM, Plus Nichrome Fuses." Recent distributions show a 92% AVG. programming yield (based on a 50% blow pattern) for these new Schottky PROM Products. All Signetics PROM products introduced since February 1974 (including the Field Programmable Logic Array) are the "second generation" TTL Schottky type.

TTL SCHOTTKY PROM FAILURE RATES/MTBF

The failure rates and MTBF (mean time between failures) for PROM devices, for fused links, and for unfused links are calculated from the data in the life test summary.

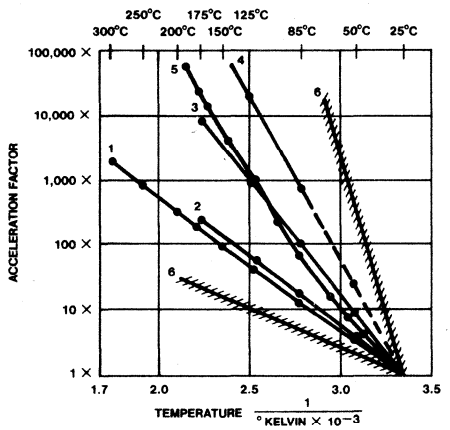
The failure rate for any given Signetics PROM can be approximated by multiplying the fuse failure rate by the number of fuses in the device and adding the result to the basic device reliability. For example, the FPLA has 1920 nichrome links. Assuming that 50% (960) are blown, we get

960 X .00000137 + 960 X.00000132 + .000893 = .00347%/1000 Hours

PROCESS	PARAMETER	FAILURE RATE(1)	MTBF = 1/F.R.
Std	Device	.000893	1.12×10^8 hours
Aluminum	Fused Link	.00000137	7.30×10^{10} hours
Schottky DLM Plus	Unfused Link	.00000132	7.58×10^{10} hours
Nichrome Fuses			

Note: The failure rate (F.R.) calculations are at 60% confidence and values are shown in % per 1000 hours. Calculations are based on the 25°C equivalent device hours (combined HTOL and HTSL).

FAILURE RATE ACCELERATION FACTOR vs TEMPERATURE CURVE (from Signetics Product Reliability Report R363)



NOTES

1. Calculated from the Signetics Failure Rate vs Temperature Graph of Figure 3.2. Signetics uses acceleration factors of 15 (for 85°C), 50 (for 125°C), 100 (for 150°C), 200 (for 175°C), 350 (for 200°C), 970 (for 250°C) and 2100 (for 300°C) to relate to 25°C equivalent ambient temperature. The 25°C to 125°C segment of the graph is based primarily on operating life data. The segment of the graph above 125°C is based on high temperature storage data. The graph equates to an "activation energy" Ea = 0.41 eV.
2. Calculated from MIL-HDBK-217B, 20 September, 1974, Table 2.1.5-4 for ITT_1 vs T_J values. The graph equates to an "activation energy" E_A = 0.41 eV and is applicable to all bipolar digital (except ECL) in the normal mode of operation.
3. Calculated from MIL-HDBK-217B, 20 September, 1974, Table 2.15-4 for ITT_2 vs T_J values. The graph equates to an "activation energy" E_A = 0.70 eV and is applicable to all MOS, all Linear, and bipolar ECL devices in the normal mode of operation.
4. Calculated from MIL-STD-883A, 15 November 1974, Figures 1005-4 and 1015-1 by extrapolating the time temperature regression graph from 78°C back to 25°C. The MIL-STD-883A graph is the Bell Telephone Laboratories Graph (Specification A-B-689143, 16 January 1974 etc.) and as such applies to storage and operating T_J values and primarily surface inversion failure mechanisms. The graph equates to an "activation energy" E_A = 1.02 eV.
5. This curved graph is the result of plotting the "rule of thumb" that failure rates (hence acceleration factors) double for every + Δ10°C.
6. All competitor data (available to Signetics) produced graphs falling within these two boundaries. The two boundaries equate to "activation energies" of E_A = 0.23 eV (for lower graph) and E_A = 1.92 eV.

82S23-F,N,W • 82S123-F,N,W

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S23 and 82S123 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, N or F, and for the military temperature range (-55°C to +125°C) specify S82S23/123, F or W.

FEATURES

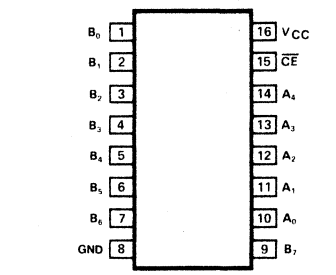
- **Address access time:**
  N82S23/123: 50ns max
  S82S23/123: 65ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S23/123: -100μA max
  S82S23/123: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S23: Open collector
  82S123: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

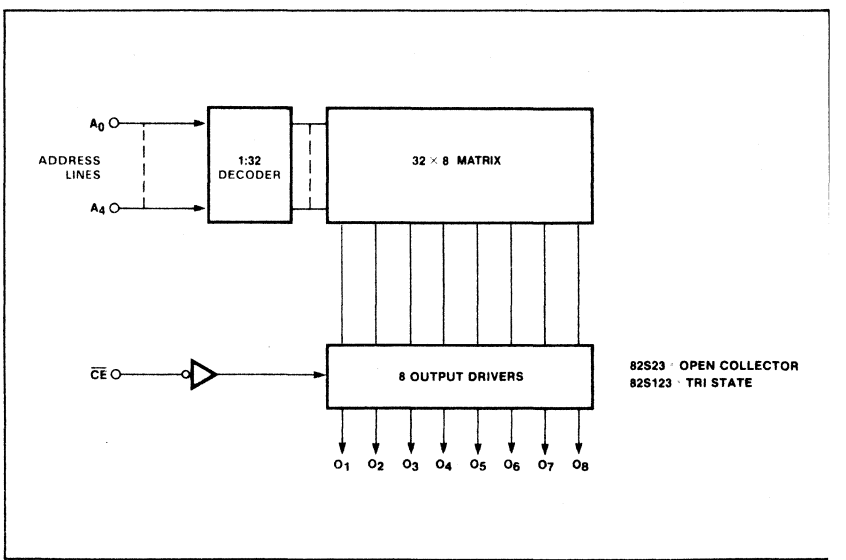
PIN CONFIGURATION

F,N,W, PACKAGE



W = Flat Pak
F = Cerdip
N = Plastic

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S23)	+5.5	
V_O	Off-state (82S123)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S23/123	0 to +75	
	S82S23/123	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S23/123: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S23/123: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S23/123			S82S23/123			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.85			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2			-1.2	
	Output voltage	$\overline{CE}$= Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			50			50	
	Output current								
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
$I_{O(OFF)}$	Hi-Z state (82S123)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
		$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-50	
I_{OS}	Short circuit (82S123)	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	-20		-90	-20		-100	mA
I_{CC}	V_{CC} supply current				77			85	mA
	Capacitance	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

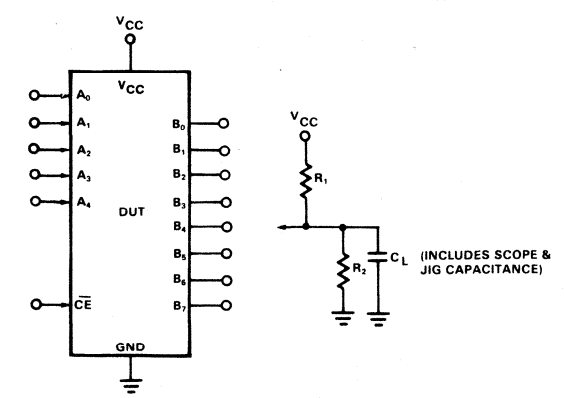
R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF[1]
N82S23/123: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S23/123: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S23/123			S82S23/123			UNIT
			Min	Typ	Max	Min	Typ	Max	
Access time									ns
T_{AA}[2]	Output	Address			50			65	
T_{CE}	Output	Chip enable			35			40	
Disable time									ns
T_{CD}	Output	Chip disable			35			40	

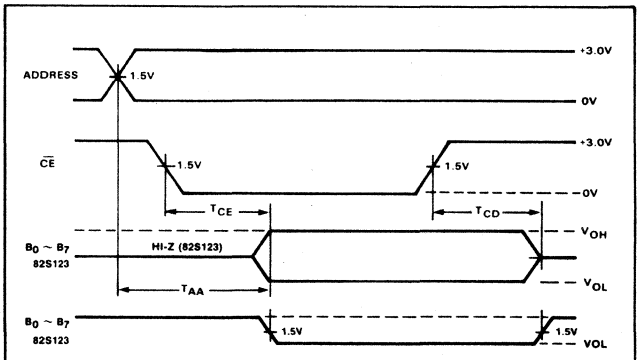
NOTES

Positive current is defined as into the terminal referenced.
Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: t_r = t_f = 5ns (10% to 90%)

10139-F,N

DESCRIPTION

The 10139 is organized as an array of 32 words and 8 bits. The initial unprogrammed state is 0 (low). The user may program 1's to obtain any desired pattern. Outputs go to the 0 (low) state when the chip enable input is high, allowing wired-OR output connections. A 50Ω output drive capability makes the part suitable for use in high performance ECL systems.

FEATURES

- **Access time: 15ns typ**
- **Power dissipation: 580mW typ**
- **Field programmable (Ni-Cr link)**
- **Fully decoded**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50Ω drive)**
- **Fully compatible with Signetics ECL 10K products**

APPLICATIONS

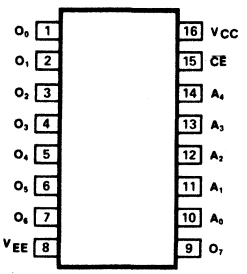
- **Programmable logic**
- **Control stores**
- **Microprogramming**
- **Hardwired algorithms**

RECOMMENDED OPERATING VOLTAGE

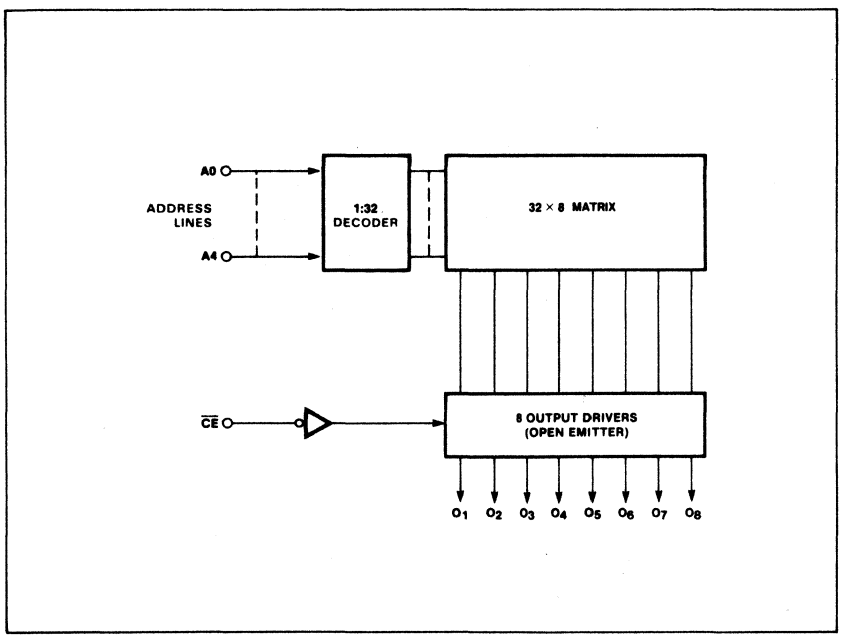
- **V_{CC} = GND, V_{EE} = -5.2V ± 5%**

PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
T_A	Temperature range Operating	-30 to +85	°C

10139-F,N

C ELECTRICAL CHARACTERISTICS[1] V_{CC} = 0V, V_{EE} = -5.2V, R_L = 50Ω to -2V

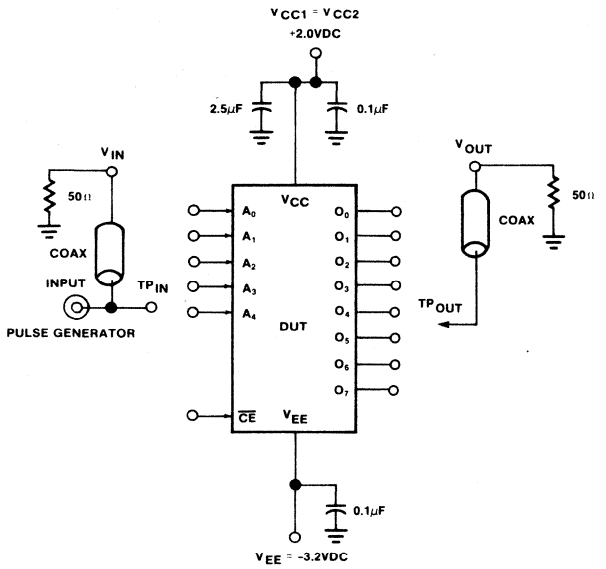
PARAMETER	TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage											V
V_{IL} Low		-1.890			-1.850			-1.825			
V_{IH} High				-0.890			-0.810			-0.700	
V_{ILA} Low threshold				-1.500			-1.475			-1.440	
V_{IHA} High threshold		-1.205			-1.105			-1.035			
Output voltage											V
V_{OL} Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.85		-1.65	-1.825		-1.615	
V_{OH} High		-1.06		-0.89	-0.96		-0.81	-0.89		-0.70	
V_{OLA} Low threshold	V_{IHA} = Min, V_{ILA} = Max			-1.655			-1.63			-1.595	
V_{OHA} High threshold		-1.08			-0.98			-0.91			
Input current											μA
I_{IL} Low	V_{IL} = Min				0.5						
I_{IH} High	V_{IH} = Max						265				
I_{EE} Power supply drain current							145				mA

C ELECTRICAL CHARACTERISTICS[1,2] V_{CC} = 2V, R_L = 50Ω to ground, -30°C ≤ T_A ≤ 85°C, V_{EE} = -3.2V

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						ns
T_{AA}	Output	Address			22	
T_{CE}	Output	Chip enable			17	
Disable time						ns
T_{CD}	Output	Chip disable			17	
Rise and fall time						ns
t_+ Rise time (20-80%)				4.0		
t_- Fall time (20-80%)				4.0		

10139-F,I

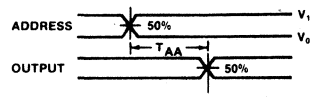
TEST LOAD CIRCUIT



Input pulse: $t_+ = t_- = 2.0 - 0.2$ns (20 to 80%)

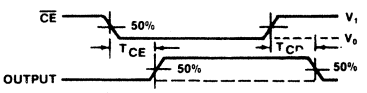
VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2$ns (20 to 80%), $t_f = 2$ns (20 to 80%)

CHIP ENABLE/DISABLE TIMES

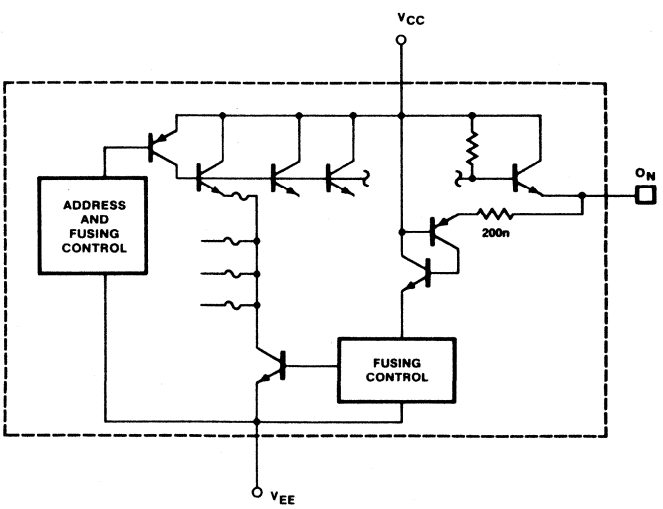


Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2$ns (20 to 80%), $t_f = 2$ns (20 to 80%)

NOTES

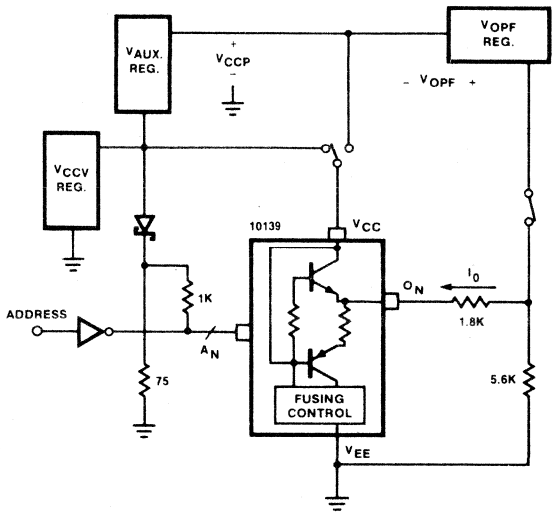
1. Dc and ac specifications apply after thermal equilibrium has been established, with transverse air flow greater than 500 linear ft/min.
2. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
3. Test procedures are shown for only 1 input or set of input conditions. Other inputs are tested in the same manner.

TYPICAL FUSING PATH

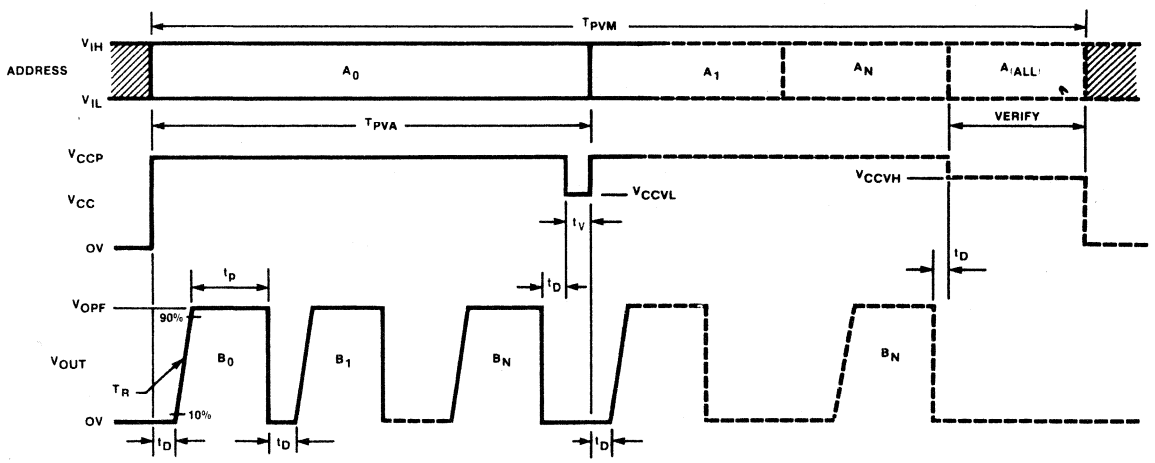


10139-F,N

YPICAL PROGRAMMING CIRCUIT



ROGRAMMING SEQUENCE



10139-F,I

PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) $T_A = +25°C$.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1,3]	I_{CCP} = 300±25mA (Transient or steady state)	11.5		12.5	
	Verify limit					V
V_{CCVH}	Upper		5.5		5.7	
V_{CCVL}	Lower		4.7		4.9	
V_S	Verify threshold[2]			V_{CCV}		V
I_{CCP}	Programming supply current	V_{CCP} = 12±.5V	275	-1.3	325	mA
	Input voltage[5]		V_{CCV}		V_{CCV}	V
V_{IH}	High		-0.8		-0.2	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = Max.			300	
I_{IL}	Low	V_{IL} = Min.			-50	
V_{OPF}	Forced Output Voltage[3,6] (program)	I_{OPF} = 2.5±.5mA (Transient or steady state)	6.0		6.8	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = 6.4±.4V	2		3	mA
T_R	Output pulse rise time		0.1		1	μs
t_p	Programming pulse width		100		125	μs
t_D	Pulse sequence delay		10			μs
t_V	Verify time		1			μs
T_{PVA}	Address program-verify cycle				2	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
5. Address buffers must be referenced to V_{CCV}.
6. V_{OPF} supply must be referenced to the V_{CCV} supply.

PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical "0" (low). To write locical "1", proceed as follows:

SET-UP

a. Set V_{EE} and $\overline{CE}$ to GND.
b. Set V_{CC} to V_{CCVH}.
c. Terminate all device outputs with a 1.8K resistor in series with a 5.6K resistor to GND.

PROGRAM-VERIFY SEQUENCE

1. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
2. After t_D delay, apply a voltage V_{OPF} to the output to be programmed via the external divider (refer to typical programming circuit). Program one output at a time.
3. After t_p delay, remove V_{OPF} from the programmed output.
4. After t_D delay, repeat steps 2 and 3 to program other bits at the same address.
5. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVH}. All programmed outputs should remain in the logic high state.
6. After t_D delay, repeat steps 1 through 5 program and verify all other address l cations.
7. After t_D delay lower V_{CC} to V_{CCVL}, ar verify all memory locations by cyclir through all device addresses.

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the programming procedure given in this data manual. The 82S126 and 82S129 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, F or N, and for the military temperature range (-55°C to +125°C) specify S82S126/129, F or R.

FEATURES

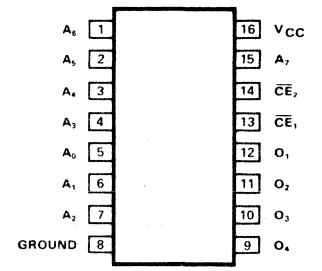
- **Address access time:**
  - **N82S126/129: 50ns max**
  - **S82S126/129: 70ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading:**
  - **N82S126/129: -100μA max**
  - **S82S126/129: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S126: Open collector**
  - **82S129: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

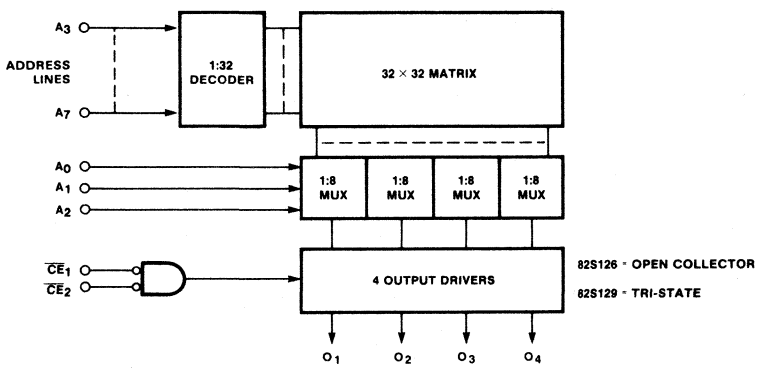
PIN CONFIGURATION

F,N,R PACKAGE*



*F = Cerdip
N = Plastic
R = Flat Pak

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S126)	+5.5	
V_O	Off-state (82S129)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S126/129	0 to +75	
	S82S126/129	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S126/129: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S126/129: -55°C ≤ T_A ≤ + 125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S126/129			S82S126/129			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2			-1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S129)	I_{OUT} = -2.0mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S129)	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, Stored high	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current				120			125	mA
	Capacitance	CE_1 or CE_2 = High V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

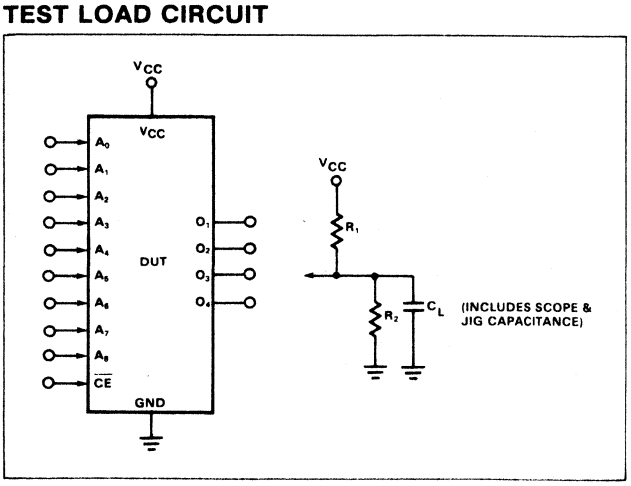
AC ELECTRICAL CHARACTERISTICS

R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF
N82S126/129: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S126/129: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

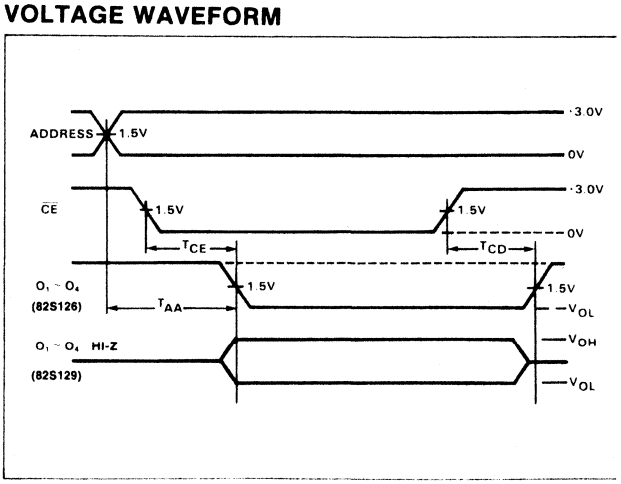
PARAMETER	TO	FROM	N82S126/129			S82S126/129			UNIT
			Min	Typ	Max	Min	Typ	Max	
Access time									ns
T_{AA}[2]	Output	Address			50			70	
T_{CE}	Output	Chip enable			25			35	
Disable time									ns
T_{CD}	Output	Chip disable			25			35	

NOTES
1. Positive current is defined as into the terminal referenced.
2. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



10149-F

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the fusing procedures given in this data sheet. The device is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 50Ω loads.

A chip enable input is provided for ease of memory expansion.

FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50kΩ drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

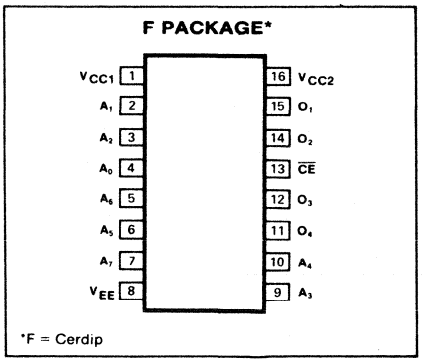
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

RECOMMENDED OPERATING RANGES

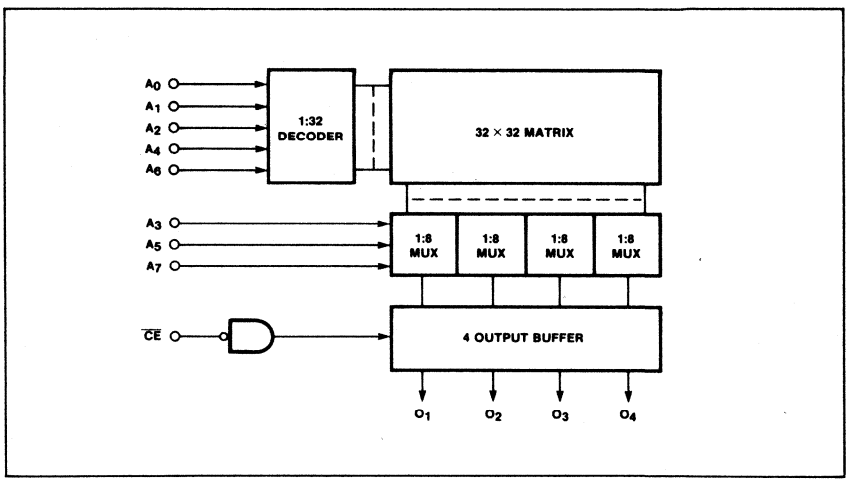
- **$V_{CC1} = V_{CC2} = GND$**
- **$V_{EE} = -5.2V \pm 5\%$**
- **$T_A = -30°C$ to $+85°C$ ambient**

PIN CONFIGURATION



*F = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	8	Vdc
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER[1]	TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage[2,3]											V
V_{IL} Low		-1.890			-1.850			-1.825			
V_{IH} High				-0.890			-0.810			-0.700	
V_{ILA} Low threshold				-1.500			-1.475			-1.440	
V_{IHA} High threshold		-1.205			-1.105			-1.035			
Output voltage											V
V_{OL} Low	V_{IH} = max	-1.89		-1.675	-1.85		-1.65	-1.825		-1.615	
V_{OH} High	V_{IL} = min	-1.06		-0.89	-0.96		-0.81	-0.89		-0.70	
V_{OLA} Low threshold	V_{IHA} = min, V_{ILA} = max			-1.655			-1.63			-1.595	
V_{OHA} High threshold		-1.08			-0.98			-0.91			
Input current											μA
I_{IL} Low	V_{IH} = max				0.5						
I_{IH} High	V_{IL} = min						265				
I_{EE} Supply drain current							150				mA

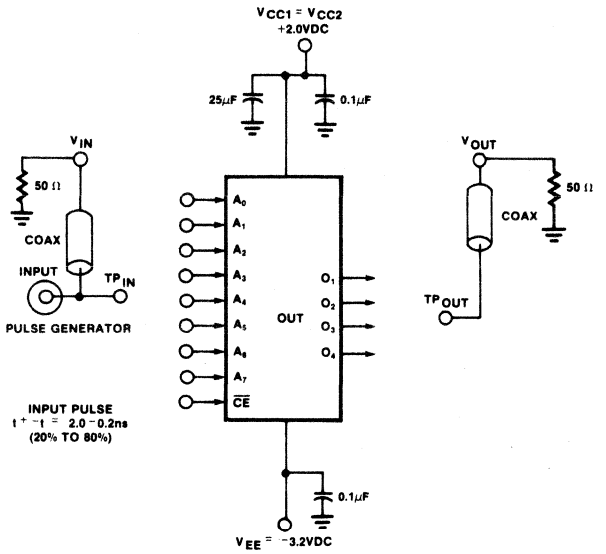
AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{EE} = -3.2V$, $V_{CC1} = V_{CC2} = 2V$, $R_L = 50\Omega$ to ground

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						ns
T_{AA}	Output	Address			20	
T_{CE}	Output	Chip enable			8	
T_{CD} Disable time	Output	Chip disable			8	ns
Rise and fall time						ns
t+ Rise time (20-80%)				4.0		
t- Fall time (20-80%)				4.0		

NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Vdc ± 1%.
3. Each ECL 10K series device has been designed to meet the dc specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to -2V.

TEST LOAD CIRCUIT



NOTES

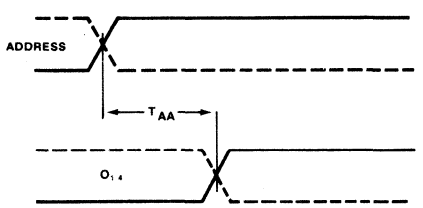
A. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.

B. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.

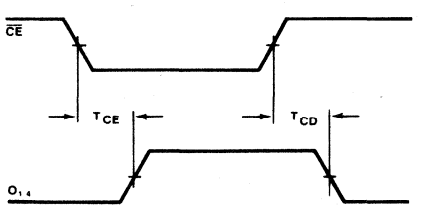
C. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE PROPAGATION DELAYS



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) $T_A = +25°C$.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1,3]	I_{CCP} = 150 ±25mA (Transient or steady state)	11.5		12.5	
	Verify limit					V
V_{CCVH}	Upper	I_{CCV} = 400 ±50mA (Transient or steady state)	5.5		5.7	
V_{CCVL}	Lower		4.7		4.9	
V_S	Verify threshold[2]			V_{CC}-1.3		V
I_{CCP}	Programming supply current	V_{CCP} = 12 ±.5V	125		175	mA
	Input voltage[5]		V_{CCV}		V_{CCV}	V
V_{IH}	High		-0.8		-0.2	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = Max.			300	
I_{IL}	Low	V_{IL} = Min.			-50	
V_{OPF}	Forced Output Voltage[3,6] (program)	I_{OPF} = 2.5±.5 mA (Transient or steady state)	6.0		6.8	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = 6.4 ±.4V	2		3	mA
T_R	Output pulse rise time		0.1		1	µs
t_p	Programming pulse width		100		125	µs
t_D	Pulse sequence delay		10			µs
t_V	Verify time		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
5. Address buffers must be referenced to the V_{CCV} supply.
6. V_{OPF} supply must be referenced to the V_{CCV} supply.

PROGRAMMING PROCEDURE

The 10149 is shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

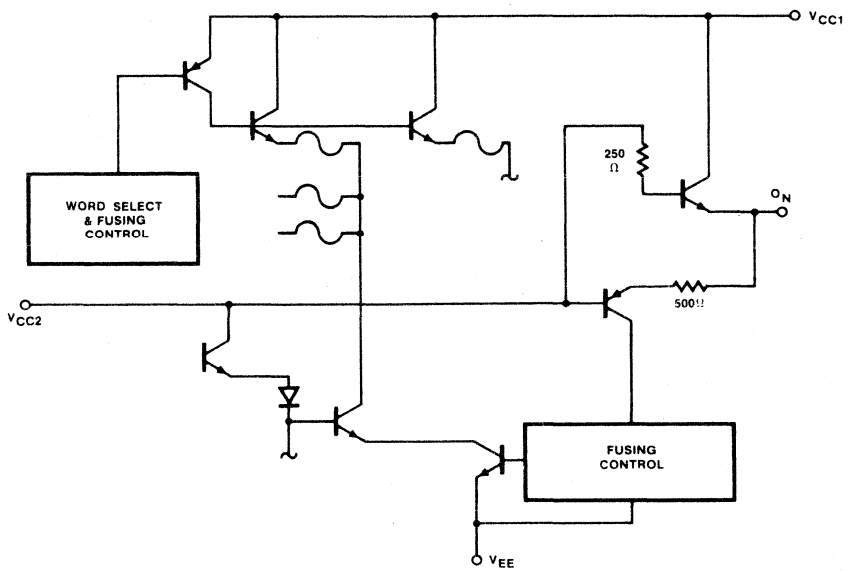
a. Set V_{EE} and $\overline{CE}$ to GND.
b. Set V_{CC1} and V_{CC2} to V_{CCVH}.
c. Terminate all device outputs with a 1.8K resistor in series with a 5.6K resistor to GND.

PROGRAM-VERIFY SEQUENCE

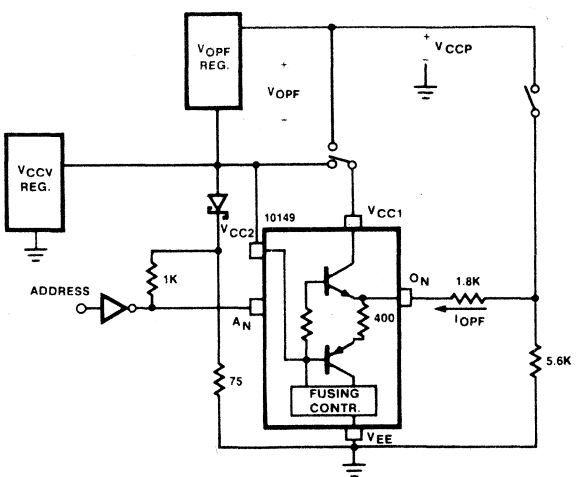
1. Select the Address to be programmed, and raise V_{CC1} to V_{CCP}.
2. After t_D delay, apply a voltage V_{OPF} to the output to be programmed via the external divider (refer to typical programming circuit). Program one output at a time.
3. After t_p delay, remove V_{OPF} from the programmed output.
4. After t_D delay, repeat steps 2 and 3 to program other bits at the same address.
5. To verify programming of all bits at the same address, after t_D delay lower V_{CC1} and V_{CC2} to V_{CCVH}. All programmed outputs should remain in the logic high state.
6. After t_D delay, repeat steps 1 through 5 to program and verify all other address locations.
7. After t_D delay lower V_{CC1} and V_{CC2} to V_{CCVL} and verify all memory locations by cycling through all device addresses.

10149-F

YPICAL FUSING PATH

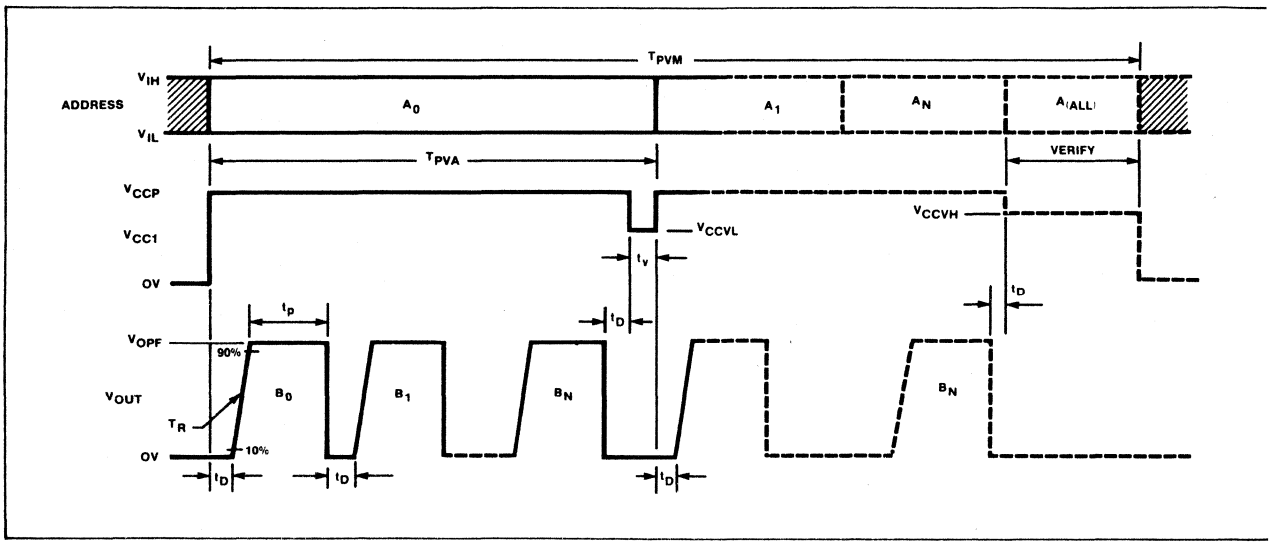


TYPICAL PROGRAMMING CIRCUIT



10149-I

PROGRAMMING SEQUENCE



82S130-F,N,R-82S131-F,N,R

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82S130/131, F or N, and for the military temperature range (–55°C to +125°C) specify S82S130/131, F or R.

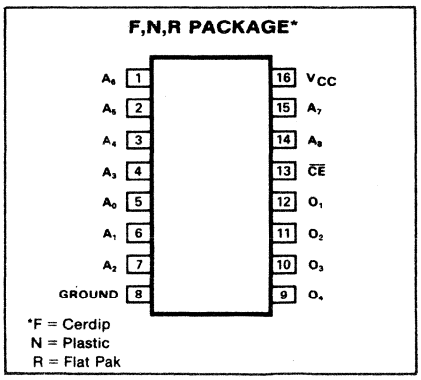
FEATURES

- **Address access time:**
  N82S130/131: 50ns max
  S82S130/131: 70ns max
- **Power dissipation: 0.3mW/bit typ**
- **Input loading:**
  N82S130/131: -100μA max
  S82S130/131: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S130: Open collector
  82S131: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

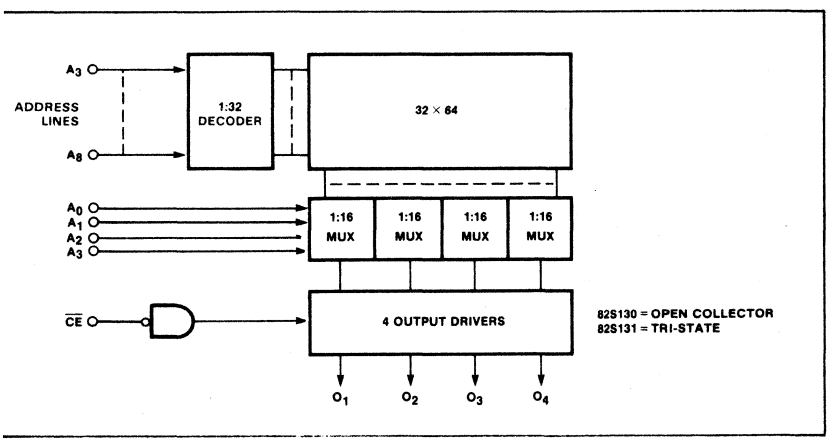
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S130)	+5.5	
V_O	Off-state (82S131)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S130/131	0 to +75	
	S82S130/131	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S130/131: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S130/131			S82S130/131			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2			-1.2	
	Output voltage	$\overline{CE}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S131)	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S130)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S131)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}$ = high, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S131)	$\overline{CE}$ = Low, V_{OUT} = 0V, Stored high	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current				140			140	mA
	Capacitance	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

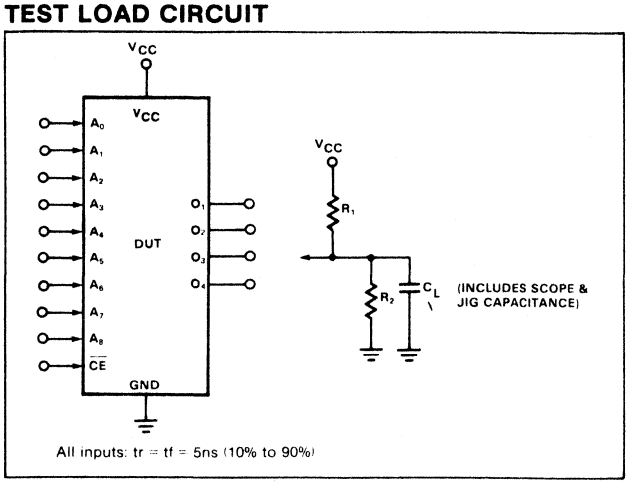
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[2]
N82S130/131: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S130/131			S82S130/131			UNIT
			Min	Typ	Max	Min	Typ	Max	
Access time									ns
T_{AA}[2]	Output	Address			50			70	
T_{CE}	Output	Chip enable			30			40	
Disable time									ns
T_{CD}	Output	Chip disable			30			40	

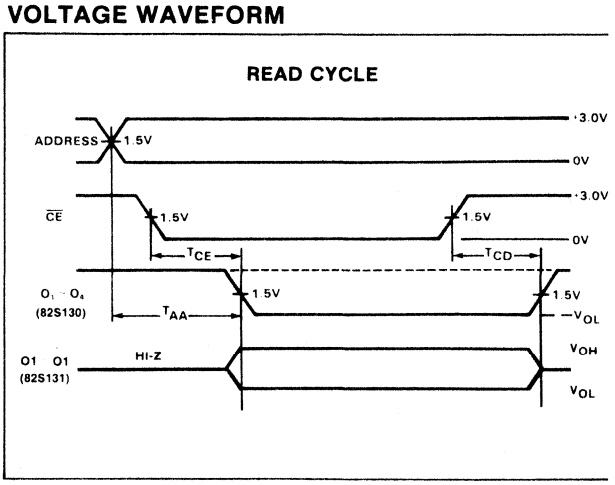
NOTES
1. Positive current is defined as into the terminal referenced.
2. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



All inputs: tr = tf = 5ns (10% to 90%)

VOLTAGE WAVEFORM



82S115-F,I,N,R

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying the binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

The 82S115 is available in the commercial and military temperature range. For the commercial temperature range (0°C to +75°C) specify N82S115, F or N, and for the military temperature range (-55°C to +125°C) specify S82S115, F, R, or I.

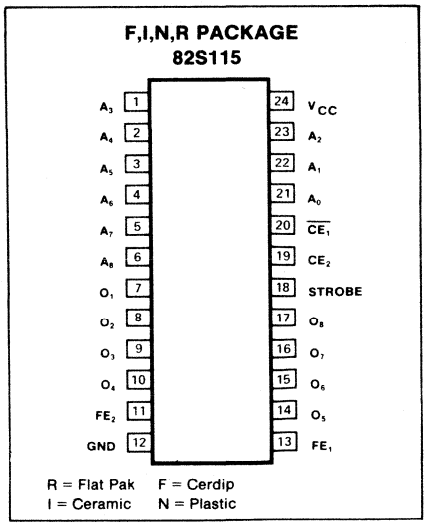
FEATURES

- **Address access time:**
  N82S115: 60ns max
  S82S115: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
  N82S115: -100μA max
  S82S115: -150μA max
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**

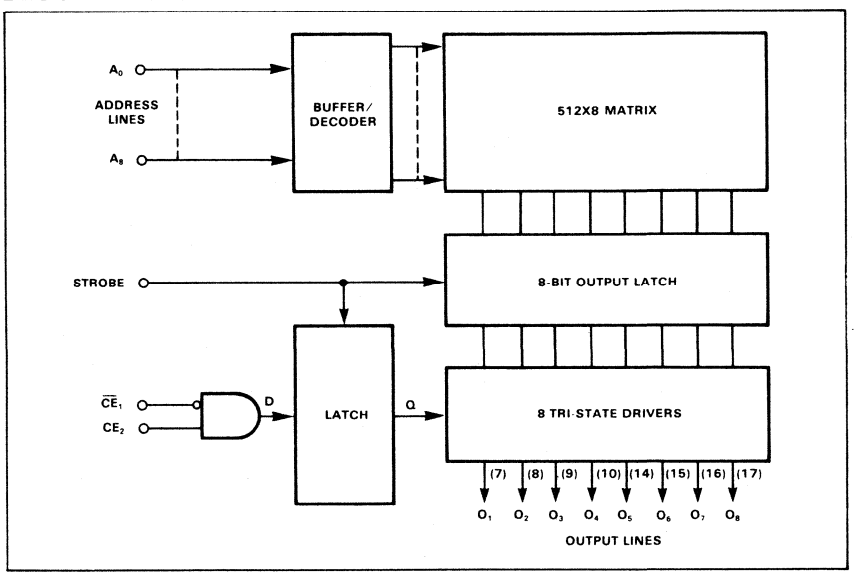
APPLICATIONS

- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S115	0 to +75	
	S82S115	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S115: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[5]	N82S115			S82S115			UNIT
			Min	Typ[8]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_1$ = Low, CE_2 = High,							V
V_{OL}	Low	I_{OUT} = 9.6mA		0.4	0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.7	3.3		2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_1$ = High or CE_2 = Low, V_{OUT} = 5.5V			40			100	μA
		$\overline{CE}_1$ = High or CE_2 = Low, V_{OUT} = 0.5V			-40			-100	
I_{OS}	Short circuit[1]	$\overline{CE}_1$ = Low, CE_2 = High, V_{OUT} = 0V, High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175			185	mA
	Capacitance	$\overline{CE}_1$ = High or CE_2 = Low, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, C_L = 30pF
N82S115: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	TEST CONDITIONS	N82S115			S82S115			UNIT
					Min	Typ[8]	Max	Min	Typ	Max	
	Access time			Latched or transparent read[2,4]							ns
T_{AA}[6]		Output	Address			40	60			90	
T_{CE}		Output	Chip enable			20	40			50	
	Disable time										ns
T_{CD}		Output	Chip disable			20	40			55	
	Setup and hold time			Latched read only[3,4]							ns
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10			15			
T_{ADH}	Hold time	Output	Address		0			5			
	Pulse width										ns
T_{SW}	Strobe				30	15		40			
	Latch time										ns
T_{SL}	Strobe				60	35		90			
	Delatch time										ns
T_{DL}	Strobe						35			45	

NOTES on following page.

)TES

No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.

If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.

In latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

During operation the fusing pins FE1 and FE2 may be grounded or left floating.

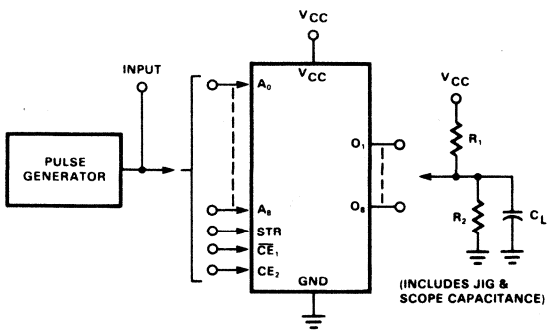
Positive current is defined as into the terminal referenced.

Tested at an address cycle time of 1μsec.

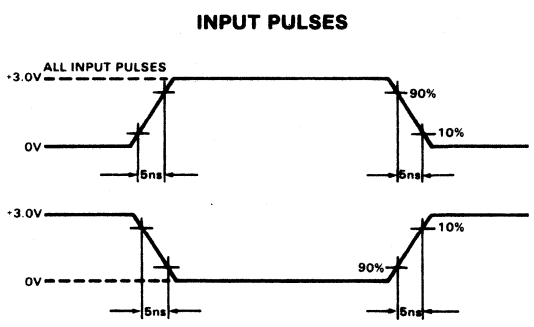
Areas shown by crosshatch are latched data from previous address.

(Typical values are at V_{CC} = 5V, T_A = 25°C)

EST LOAD CIRCUIT

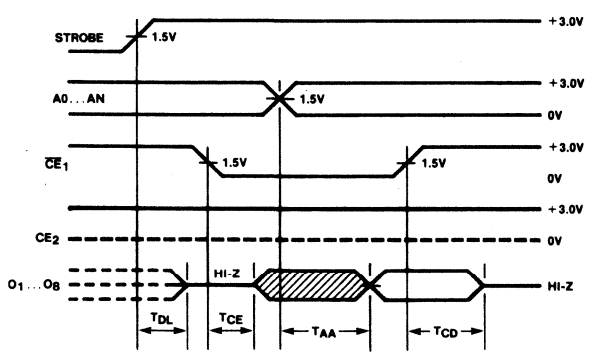


VOLTAGE WAVEFORM



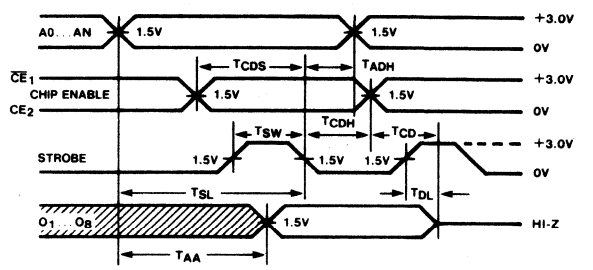
IMING DIAGRAMS

TRANSPARENT READ[2,7]



Output Latches Not Used

LATCHED READ[3,7]



Output Latches Used

PROGRAMMING SYSTEM SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 200 ± 25mA, Transient or steady state	4.75		5.25	
I_{CCP}	Programming supply current	V_{CCP} = +5.0 ± .25V	175	200	225	mA
	Verify limit					V
V_{CCVH}	Upper		5.3	5.5	5.7	
V_{CCVL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
	Input voltage					V
V_{IL}	Low		0		0.8	
V_{IH}	High		2.4		5.5	
	Input Voltage (FE_1 & FE_2)					
V_{ILP}	Low				0.5	
V_{IHP}	High		4.5	5.0	5.5	
	Input current (FE_1 & FE_2 only)					
I_{IL}	Low	V_{IL} = +0.45V			-100	μA
I_{IH}	High	V_{IH} = +5.5V			10	mA
	Input current (except FE_1 & FE_2)					μA
I_{IL}	Low	V_{IL} = +0.45V			-100	
I_{IH}	High	V_{IH} = +5.5V			25	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Output current (program)[5]	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10		50	μs
t_P	FE_2 programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	V_{CC} = V_{CCP}			12	sec
T_{PS}	Programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 3ms.
5. I_{OFF} is monitored as the peak programming current, abnormal fusing occurs when I_{OFF} < MIN or I_{OFF} > MAX.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S115 is shipped with all bits at logical low. To write logical high, proceed as follows:

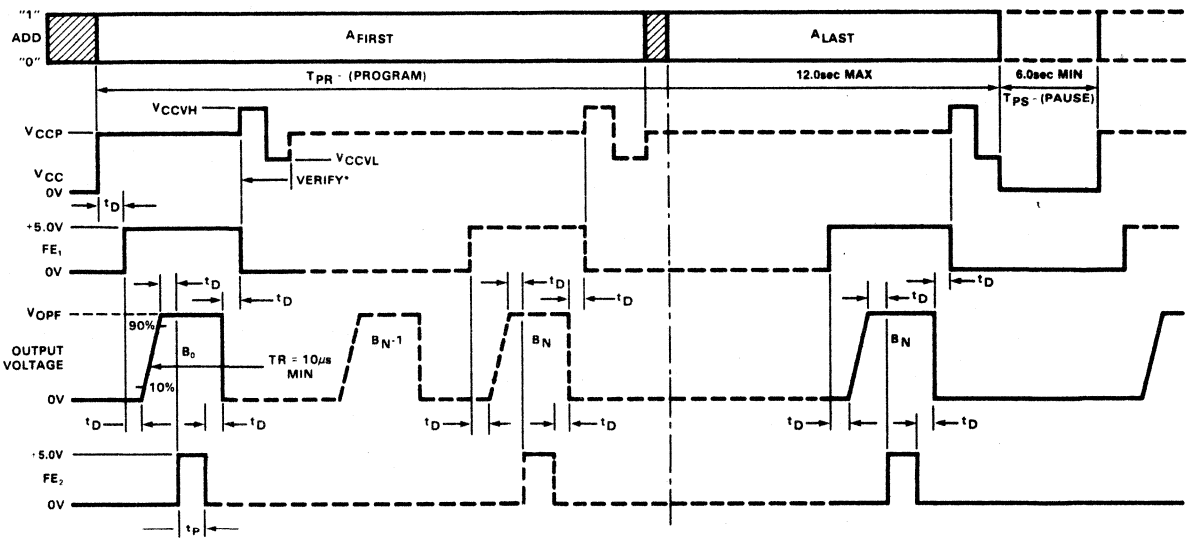
SET-UP

1. Apply GND to pin 12.
2. Terminate all device outputs with a 10KΩ resistor to V_{CC}. (Optional used for compatibility with Signetics generic programming procedure).
3. Set $\overline{CE}_1$ to logic low, and CE_2 to logic high (TTL levels).
4. Set Strobe to logic high level.

Program-Verify Sequence

1. Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
2. After t_D delay, apply to FE_1 (pin 13) a voltage source of V_{IHP}, with 10mA sourcing current capability.
3. After t_D delay, apply a voltage source of V_{OPF} to the output to be programmed. Program one output at a time.
4. After t_D delay, raise FE_2 (pin 11) from V_{ILP} to V_{IHP} for a period of t_P, and then return to V_{ILP}. Pulse source must have a 10mA sourcing current capability.
5. After t_D delay, remove +17.0V suppl from programmed output.
6. To verify programming, after t_D delay return FE_1 to V_{ILP}. Raise V_{CC} to V_{CCH}. Th programmed output should remain in th high state. Again, lower V_{CC} to V_{CCL}, an verify that the programmed output re mains in the high state.
7. Raise V_{CC} to V_{CCP} and repeat steps through 6 to program other bits at th same address.
8. Repeat steps 1 through 7 to program a other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S141-F,N,F

DESCRIPTION

The 82S141 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S141 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S141 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S141, F or N, and for the military temperature range (–55°C to +125°C) specify S82S141, F, or R.

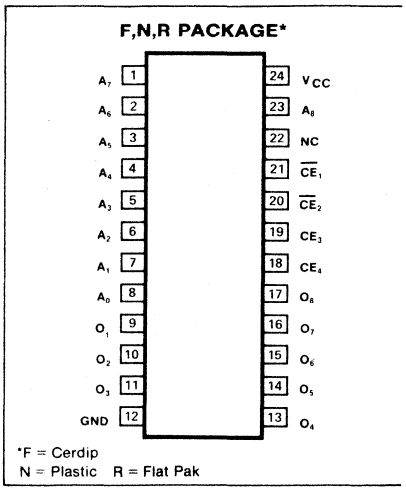
FEATURES

- **Address access time:**
  N82S141: 60ns max
  S82S141: 90ns max
- **Power dissipation: .17mW/bit typ**
- **Input loading:**
  N82S141: –100μA max
  S82S141: –150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

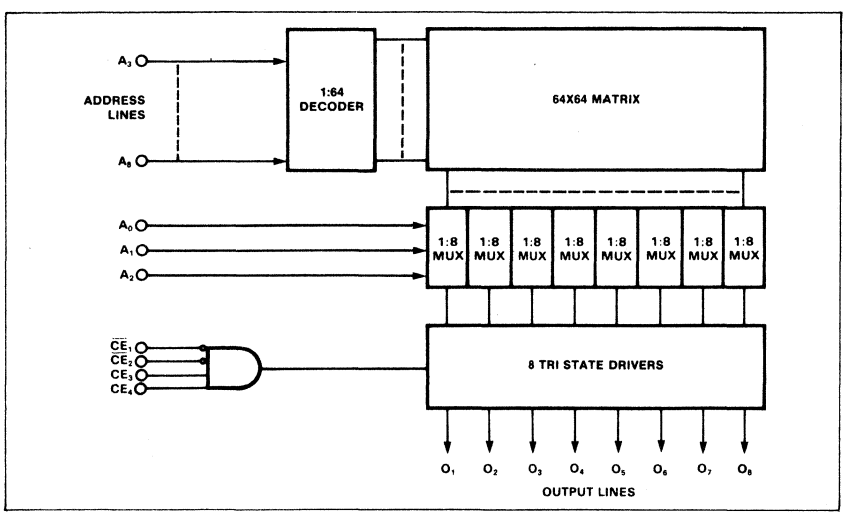
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



*F = Cerdip
N = Plastic R = Flat Pak

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S141	0 to +75	
	S82S141	-55 to +125	
T_{STG}	Storage	-65 to +150	

C ELECTRICAL CHARACTERISTICS

N82S141: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

	PARAMETER	TEST CONDITIONS[1]	N82S141			S82S141			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2			-1.2	
	Output voltage								V
V_{OL}	Low	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, I_{OUT} = -2.0mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_{1,2}$ = High or $CE_{3,4}$ = Low, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}_{1,2}$ = High or $CE_{3,4}$ = Low, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_{OUT} = 0V, High stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current				175			185	mA
	Capacitance								pF
C_{IN}	Input	$\overline{CE}_{1,2}$ = High or $CE_{3,4}$ = Low, V_{CC} = 5.0V, V_{IN} = 2.0V, V_{OUT} = 2.0V		5			5		
C_{OUT}	Output			8			8		

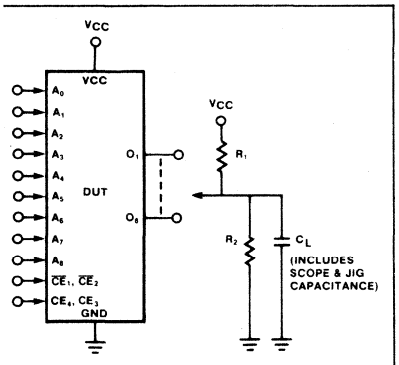
AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S141: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

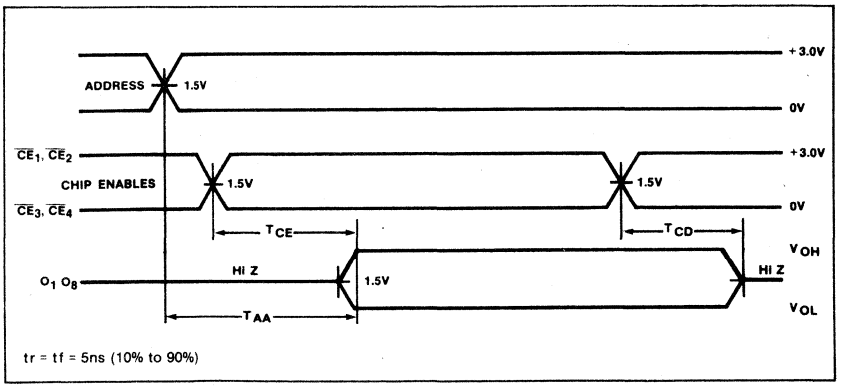
PARAMETER	TO	FROM	N82S141			S82S141			UNIT
			Min	Typ	Max	Min	Typ	Max	
Access time									ns
T_{AA}[2]	Output	Address			60			90	
T_{CE}	Output	Chip enable			40			50	
Disable time									ns
T_{CD}	Output	Chip disable			40			50	

NOTES
1. Positive current is defined as into the terminal referenced. 2. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82HS147-F,I

DESCRIPTION

The 82HS147 is field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82HS147 includes on-chip decoding and one chip enable input for ease of memory expansion, and features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS147 device is available in the commercial temperature range (0°C to +75°C), and is specified as N82HS147, F, N.

FEATURES

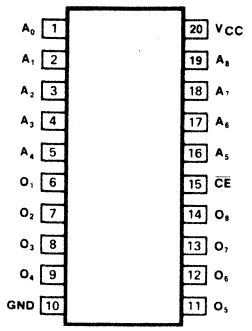
- **Address access time: 45ns max**
- **Power dissipation: 853mW max**
- **Input loading: -100μA max**
- **One chip enable input**
- **On chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

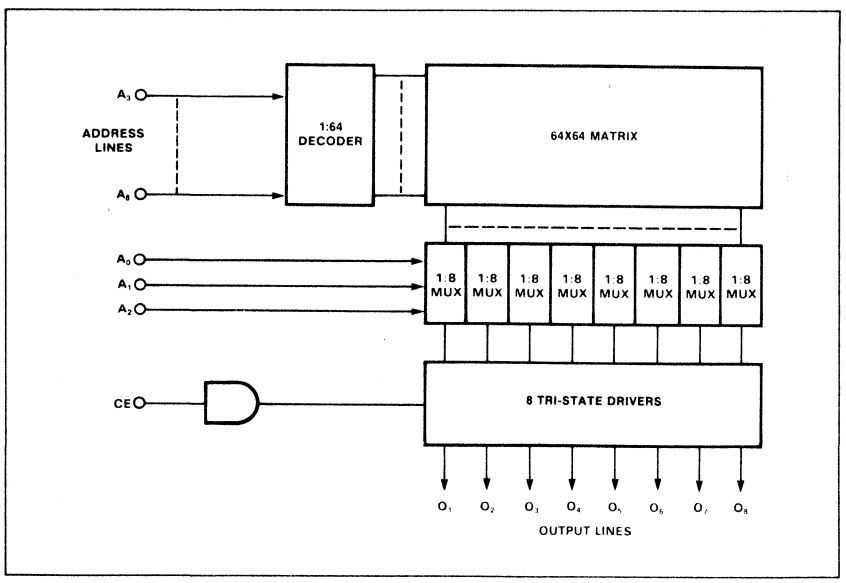
PIN CONFIGURATION

F PACKAGE



F = Cerdip N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	°C
	Temperature range		
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

)C ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$.

PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[2]					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2	
	Output voltage					V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	
V_{OH}	High	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-100	
I_{IH}	High	V_{IN} = 5.5V			40	
	Output current					
I_{OLK}	Leakage	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit[3]	V_{OUT} = 0V	-20		-70	mA
I_{CC}	V_{CC} supply current				155	mA
	Capacitance	V_{CC} = 5.0V $\overline{CE}$ = High				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

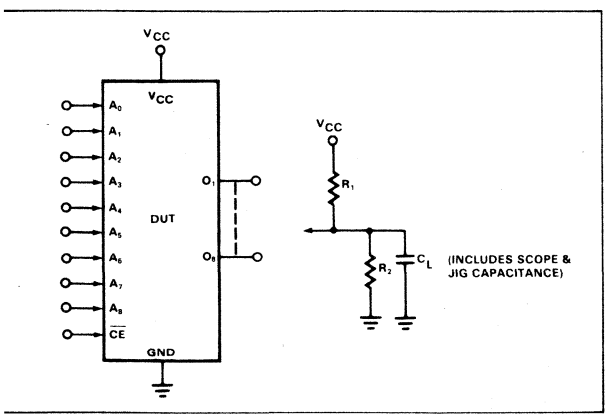
\C ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Access time						ns
T_{AA}[4]		Output	Address			45	
T_{CE}		Output	Chip enable			30	
T_{CD}	Disable time	Output	Chip disable			30	ns

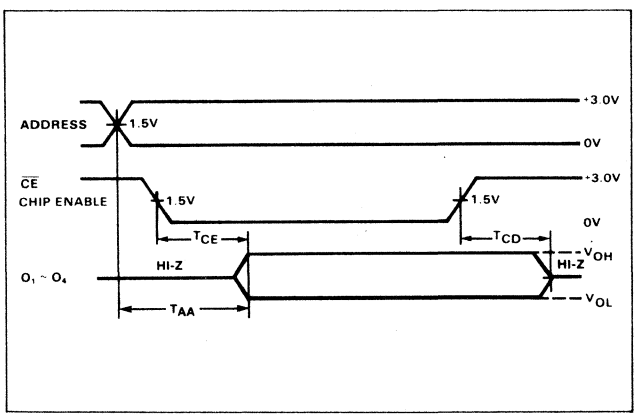
IOTES

. Positive current is defined as into the terminal referenced.
. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second
4. Tested at an address cycle time of 1μ sec.

'EST LOAD CIRCUIT



VOLTAGE WAVEFORM



BIPOLAR MEMORY

82S137-F,N,R

DESCRIPTION

The 82S137 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S137 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

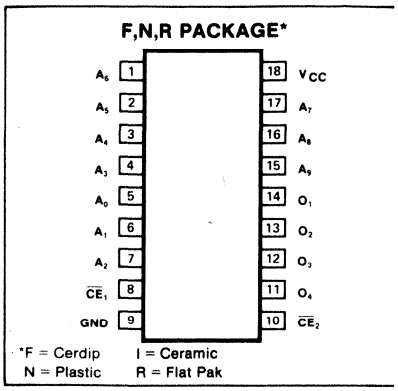
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations.

The 82S137 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S137, F or N, and for the military temperature range (–55°C to +125°C) specify S82S137, F,R, or I.

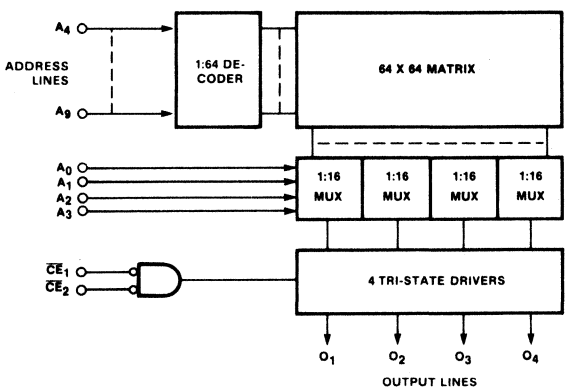
FEATURES

- **Address access time:**
  N82S137: 60ns max
  S82S137: 80ns max
- **Power dissipation: .13mW/bit typ**
- **Input loading:**
  N82S137: –100μA max
  S82S137: –150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state (82S137)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S137	0 to +75	
	S82S137	-55 to +125	
T_{STG}	Storage	-65 to +150	

C ELECTRICAL CHARACTERISTICS

N82S137; N82S137A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S137; S82S137A: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S137/137A			S82S137/137A			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2			-1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
					40			60	μA
$I_{O(OFF)}$	Off-state	$\overline{CE}_{1,2}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}_{1,2}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, Stored high	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current				140			140	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

ıC ELECTRICAL CHARACTERISTICS

R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF[1]
N82S137; N82S137A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S137; S82S137A: -55°C ≤ T_A ≤ +125°C 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S137			S82S137		
			Min	Typ	Max	Min	Typ	Max
Access time								
T_{AA}	Output	Address			60			80
T_{CE}	Output	Chip enable			30			40
Disable time								
T_{CD}	Output	Chip disable			30			40

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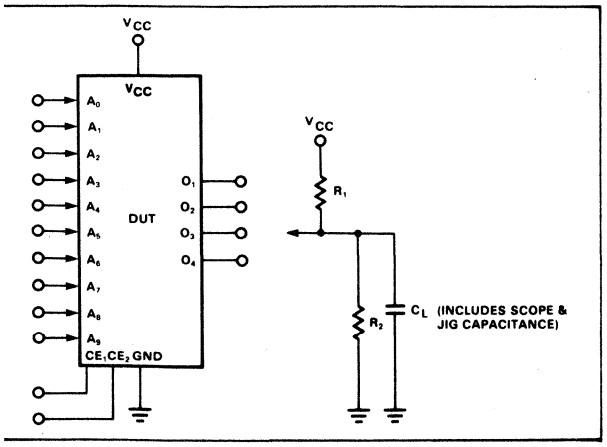
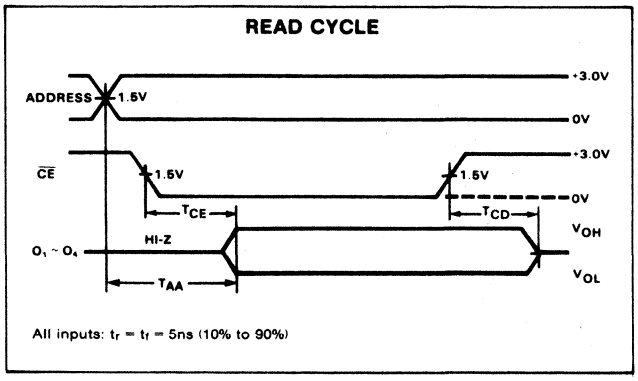
Positive current is defined as into the terminal referenced.

EST LOAD CIRCUIT



VOLTAGE WAVEFORM



82HS137I-F,N,

DESCRIPTION

The 82HS137 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82HS137 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

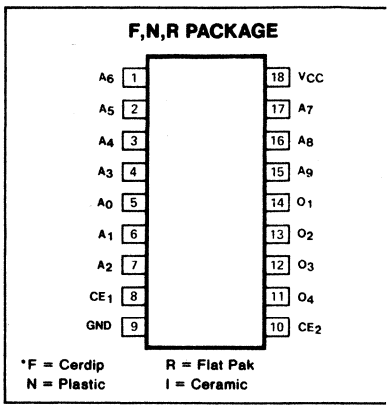
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations.

The 82HS137 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82HS137, F or N, and for the military temperature range (-55°C to +125°C) specify S82HS137, I, F, or R.

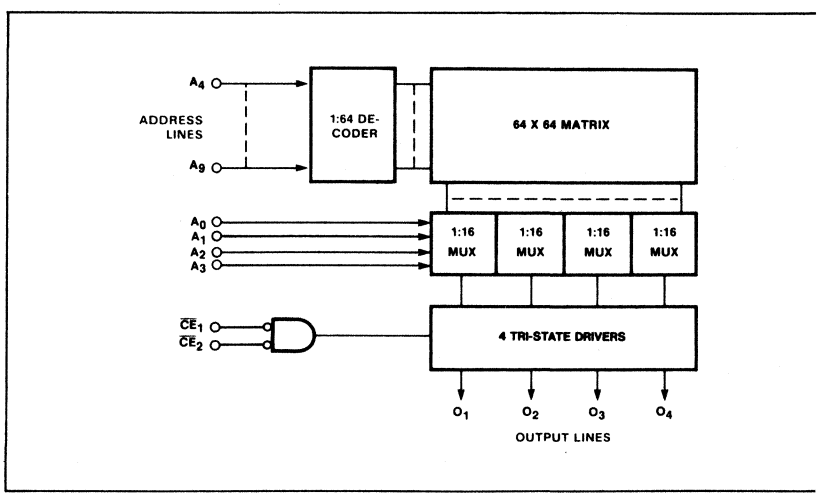
FEATURES

- **Address access time:**
  N82HS137: 45ns max
  S82HS137: 70ns max
- **Power dissipation: 13mW/bit typ**
- **Input loading:**
  N82HS137: −100μA max
  S82HS137: −150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82HS137	0 to +75	
	S82HS137	−55 to +125	
T_{STG}	Storage	−65 to +150	

C ELECTRICAL CHARACTERISTICS

N82HS137: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82HS137: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82HS137			S82HS137			UNIT
			Min	Typ[2]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2			−1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low							V
V_{OL}	Low	$I_{OUT} = 16mA$			0.45			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_{1,2}$ = High, $V_{OUT} = 0.5V$			40			60	μA
		$\overline{CE}_{1,2}$ = High, $V_{OUT} = 5.5V$			−40			−60	μA
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V,			40			60	
		Stored High	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current			85	140			150	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

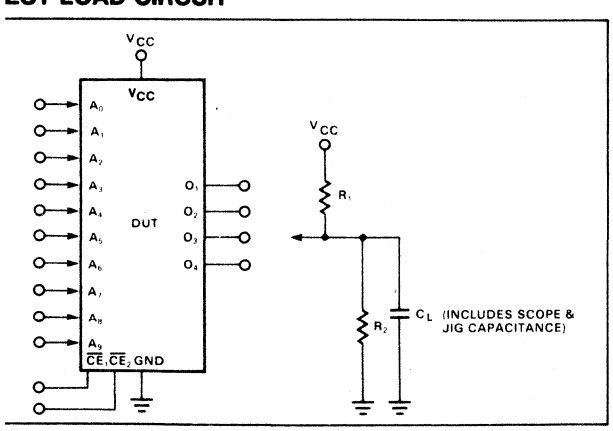
C ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[1]
N82HS137: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S137; S82S137A: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

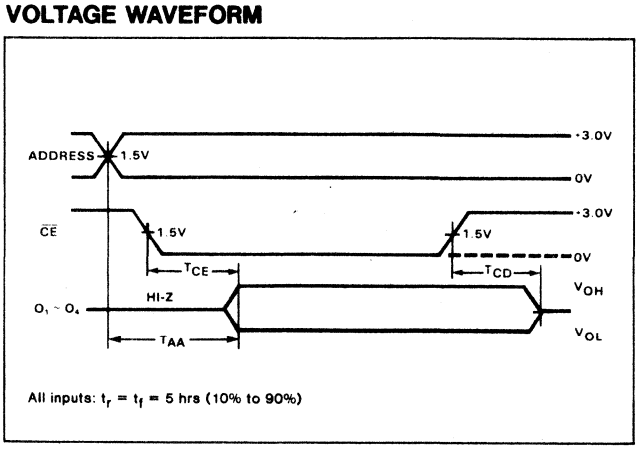
PARAMETER	TO	FROM	N82HS137			S82HS137			UNIT
			Min	Typ[2]	Max	Min	Typ	Max	
Access time									ns
T_{AA}	Output	Address		35	45			70	
T_{CE}	Output	Chip enable		15	30			40	
Disable time									ns
T_{CD}	Output	Chip disable		15	30			40	

Note
1. Positive current is defined as into the terminal referenced.
2. Typicals are at Room Temperature 5V.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S180-F,N,R,G,I • 82S181-F,N,R,G

DESCRIPTION

The 82S180 and 82S181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S180 and 82S181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of work expansion in bused organizations.

The 82S180 and 82S181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S180/181 I, F or N, and for the military temperature range (-55°C to +125°C) specify S82S180/181, R, F, G, I.

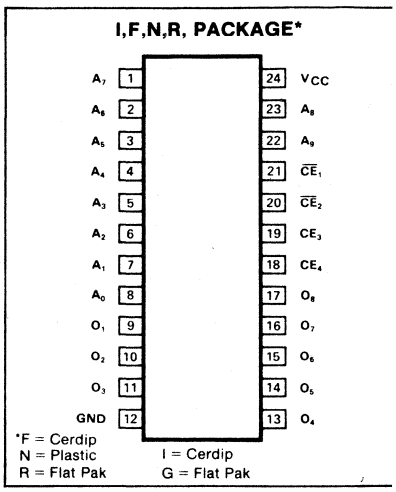
FEATURES

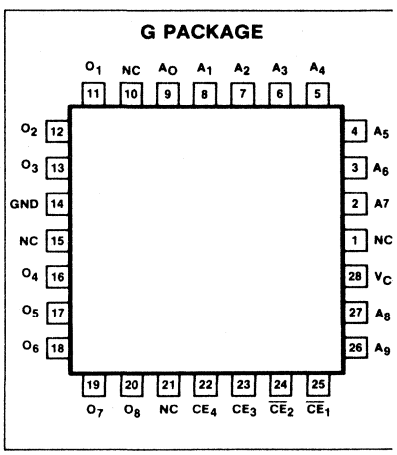
- **Address access time:**
  N82S180/181: 70ns max
  S82S180/181: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  N82S180/181: -100μA max
  S82S180/181: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S180: Open collector
  82S181: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

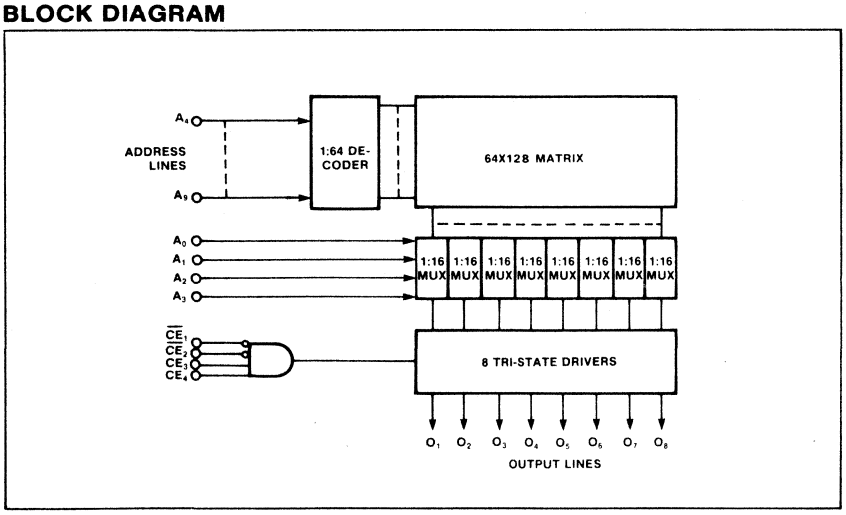
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state (82S181)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S180/181	0 to +75	
	S82S180/181	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S181: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S181			S82S181			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High							V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OLK}	Leakage (82S180)	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$			40			60	
$I_{O(OFF)}$	Hi-Z state (82S181)	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$			40			-60	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 0.5V$			-40			60	μA
I_{OS}	Short circuit 82S181	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High		125	175			185	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

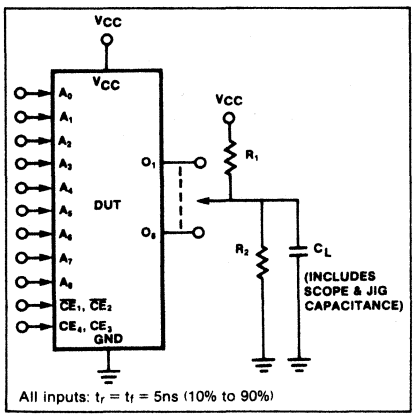
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S181: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S181			S82S181			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[2]	Output	Address		50	70			90	
T_{CE}	Output	Chip enable		20	40			50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40			50	

NOTES

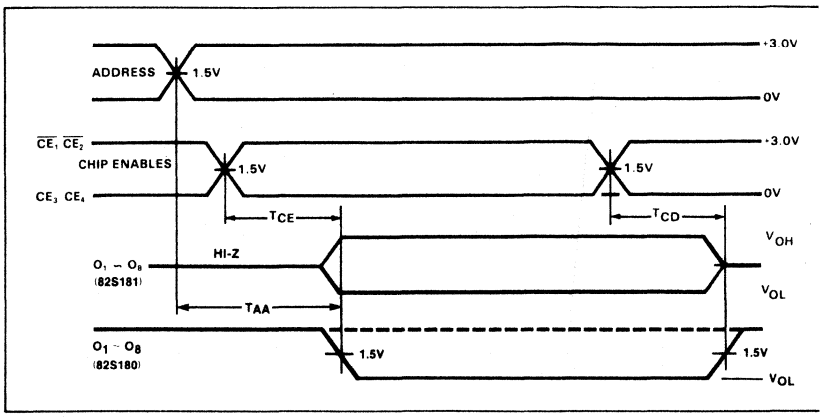
1. Positive current is defined as into the terminal referenced.
2. Tested at an address cycle time of 1μsec.
3. Typical values are $V_{CC} = 5V$, $T_A = +25$

TEST LOAD CIRCUIT



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

VOLTAGE WAVEFORM



PRELIMINARY DATA SHEET 82HS181-F,N,R,G,I

DESCRIPTION

The 82HS181 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82HS181 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a NiCr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of work expansion in bused organizations.

The 82HS181 is available in both the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82HS181 I, F or N, and for the military temperature range (–55°C to +125°C) specify S82HS181, R, F, G, I.

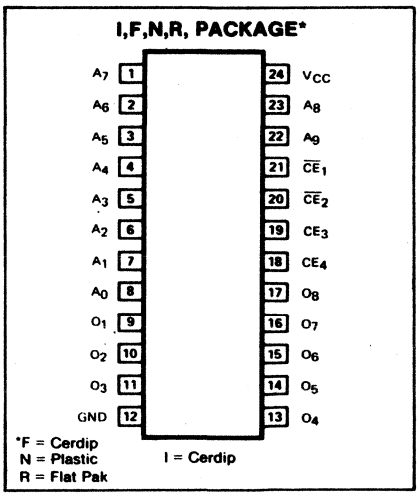
FEATURES

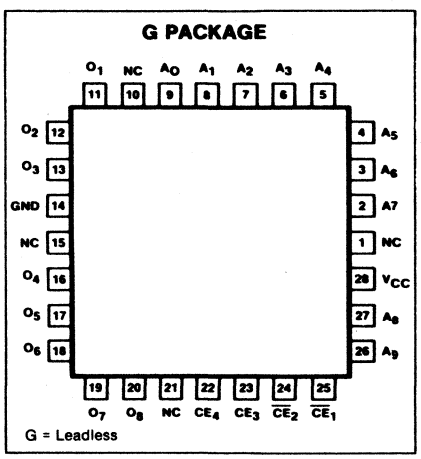
- Address access time:
  N82HS181: 55ns max
  S82HS181 : 80ns max
- Power dissipation: 85μW/bit typ
- Input loading:
  N82HS181 : –100μA max
  S82HS181 : –150μA max
- On-chip address decoding
- Output options:
  82HS181 : Tri-State
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

APPLICATIONS

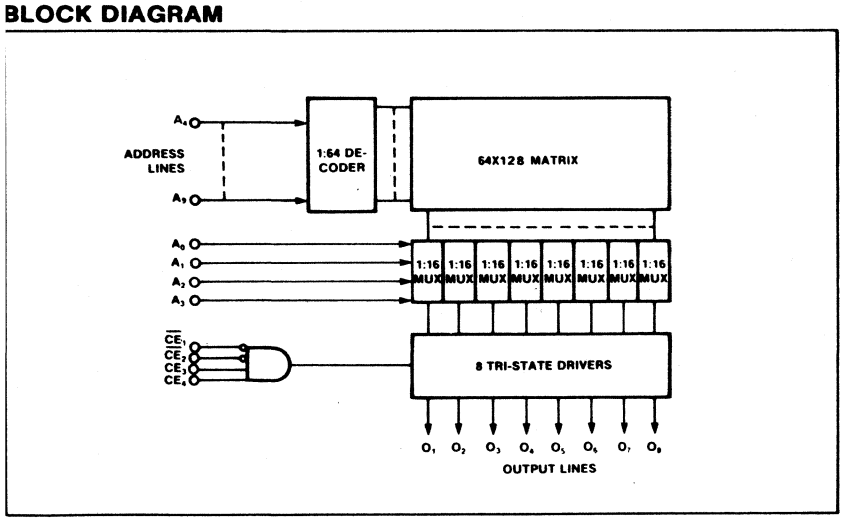
- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82HS181	0 to +75	
	S82HS181	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82HS181: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82HS181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82HS181:			S82HS181:			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}									
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{OUT} = 5.5V			40			-60	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{OUT} = 0.5V			-40			60	μA
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_{OUT} = 0V High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High		125	175			185	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

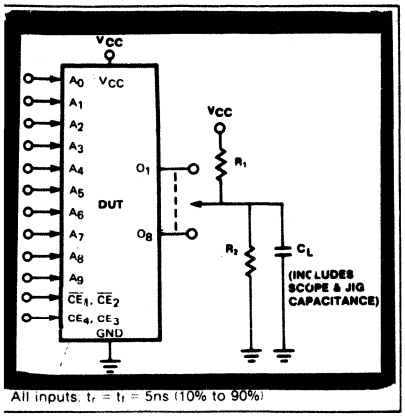
R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82HS181: 0°C ≤ T_A ≤ +75°C; 4.75V ≤ V_{CC} ≤ 5.25V
S82HS181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82HS181:			S82HS181:			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[2]	Output	Address		45	55			80	
T_{CE}	Output	Chip enable		20	35			45	
Disable time									ns
T_{CD}	Output	Chip disable		20	35			45	

NOTES

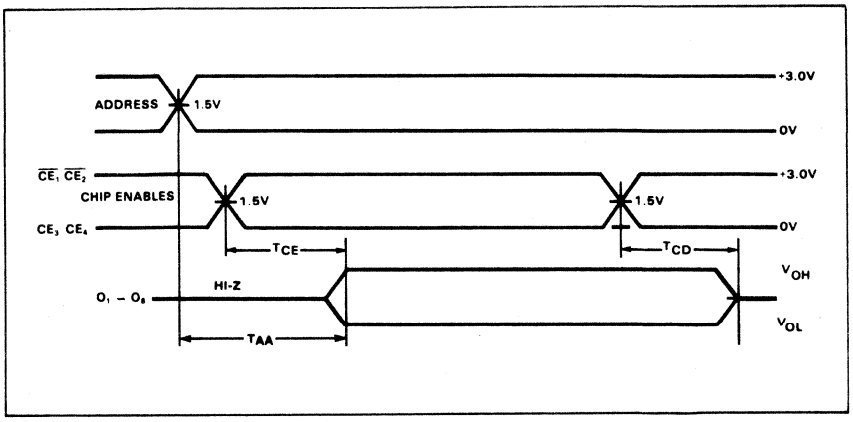
1. Positive current is defined as into the terminal referenced.
2. Tested at an address cycle time of 1μsec.
3. Typical values are V_{CC} = 5V, T_A = +25

TEST LOAD CIRCUIT



All inputs. $t_r = t_f = 5ns$ (10% to 90%)

VOLTAGE WAVEFORM



82LS181-F,G,N,R

DESCRIPTION

The 82LS181 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82LS181 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82LS181 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82LS181, F or N, and for the military temperature range (−55°C to +125°C) specify S82LS181, F,G, or R.

FEATURES

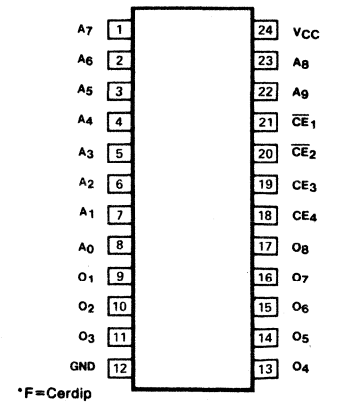
- **Address access time:**
  N82LS181: 120ns max
  S82LS181: 180ns max
- **Power dissipation: 37μW/bit typ**
- **Input loading:**
  N82LS181: −100μA max
  S82LS181: −150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

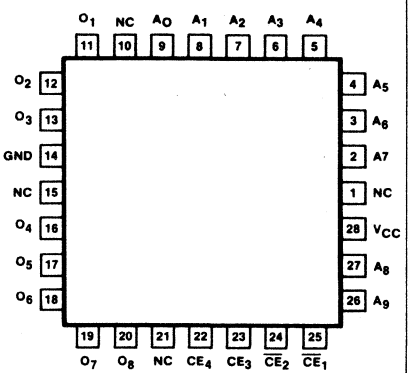
PIN CONFIGURATION

F,G,N,R PACKAGE*

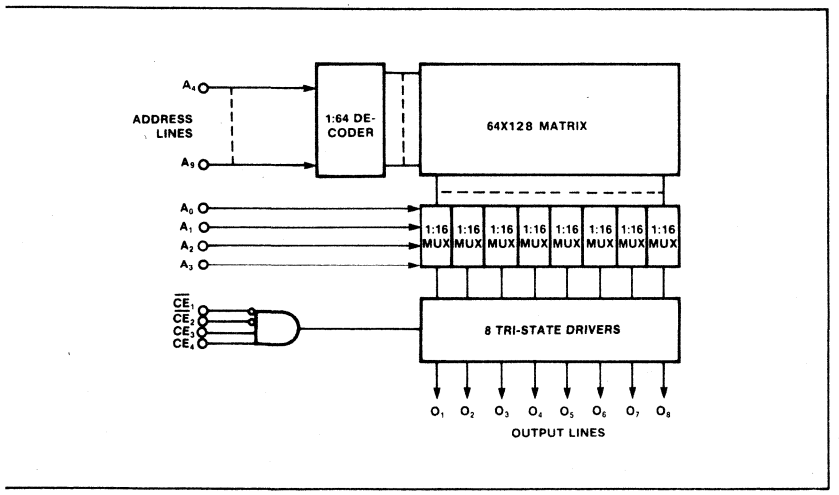


*F=Cerdip
N = Plastic
R = Flat package

G PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state (82LS181)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82LS181	0 to +75	
	S82LS181	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82LS181: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS181: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82LS181			S82LS181			UNIT
			Min	Typ[2]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2			−1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High							V
V_{OL}	Low	$I_{OUT} = 4.8mA$			0.45			0.5	
V_{OH}	High	$I_{OUT} = -1mA$	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low $V_{OUT} = 5.5V$			−40			−60	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low $V_{OUT} = 0.5V$			40			60	μA
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ high stored	−10		−70	−10		−85	mA
I_{CC}	V_{CC} supply current			60	80			85	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

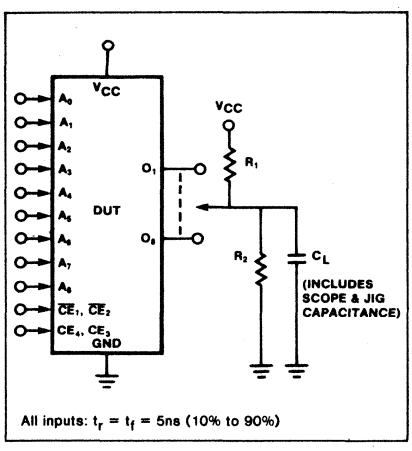
$R_1 = 1k\Omega$, $R_2 = 2k\Omega$, $C_L = 30pF$
N82LS181: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS181: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	N82LS181			S82LS181			UNIT
				Min	Typ[2]	Max	Min	Typ	Max	
	Access time									ns
T_{AA}		Output	Address		100	120			180	
T_{CE}		Output	Chip enable		35	50			70	
	Disable time									ns
T_{CD}		Output	Chip disable		35	50			70	

NOTES

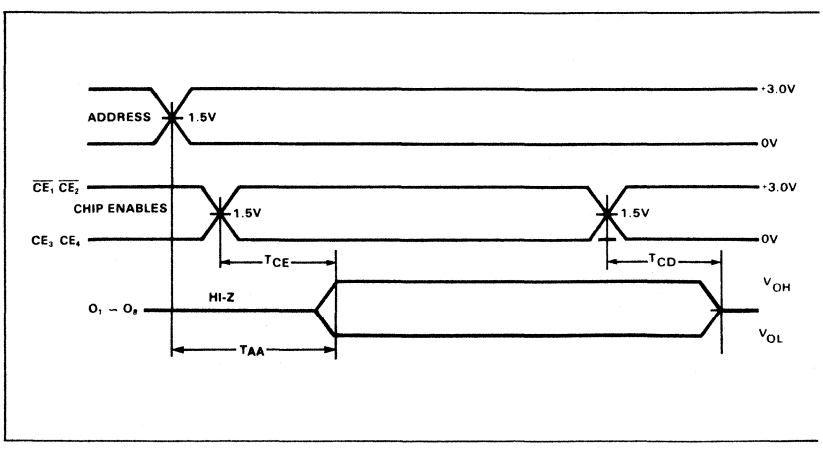
1. Positive current is defined as into the terminal referenced. 2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

TEST LOAD CIRCUIT



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

VOLTAGE WAVEFORM



82PS181-F,N,G,R

DESCRIPTION

The 82PS181 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82PS181 is programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include the decoding of 4 chip enable inputs for ease of memory expansion and also for the control of an on-chip power strobe. When the device is deselected not only are the device outputs turned off but a standby power mode reduces power dissipation over 95%. The three-state (82PS181) output organization is available for optimization of word expansion in bused memory structures.

The 82PS181 is available in both commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82PS181F or N, and for the military temperature range (−55°C to +125°C) specify S82PS181F,G,R.

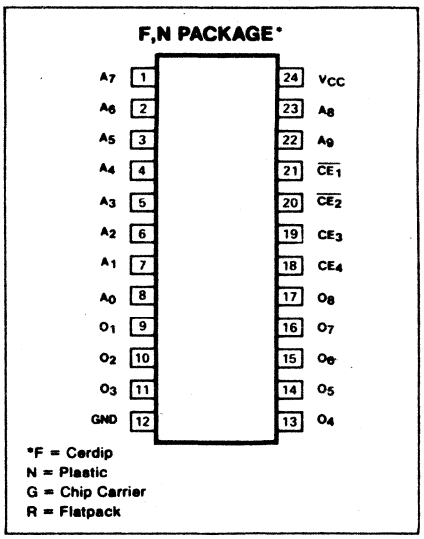
FEATURES

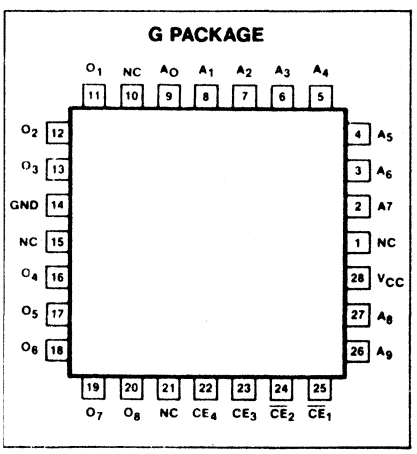
- **Address access time:**
  N82PS181: 70ns max
  S82PS181: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  N82PS181: −100μA max
  S82PS181: −150μA max
- **On-chip address decoding**
- **Output**
  82PS181: three-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**
- **6mA typ standby current**

APPLICATIONS

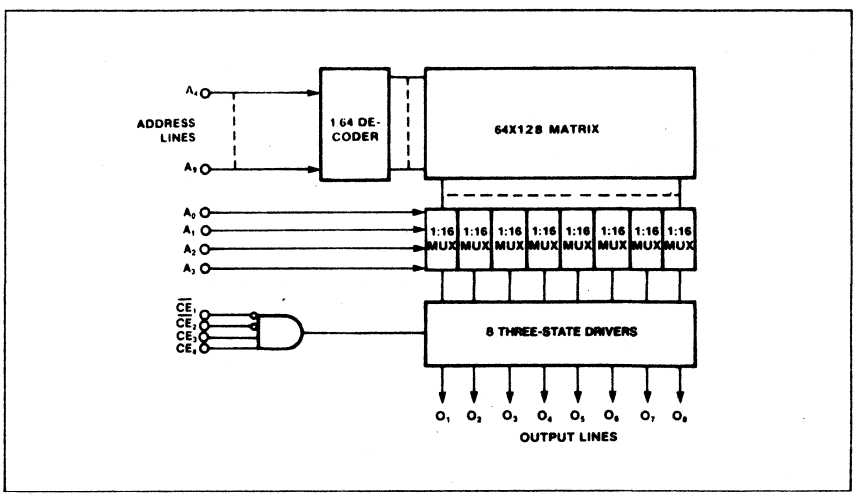
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state (82PS181)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82PS181	0 to +75	
	S82PS181	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82PS181: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82PS181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

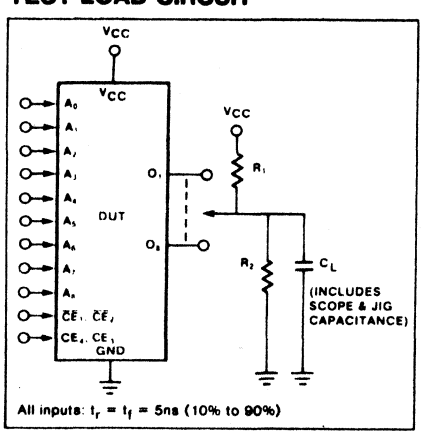
PARAMETER		TEST CONDITIONS	N82PS181			S82PS181			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$			−1.2			−1.2	
	Output voltage								V
V_{OL}	Low				0.45			0.5	
V_{OH}	High (82PS181)		2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state (82PS181)				−40			−60	μA
I_{OS}	Short circuit (82PS181)		−20		−70	−15		−85	mA
I_{CCS}	Standby V_{CC} supply current	$\overline{CE}_{1,2}$ = High or $CE_{3,4}$ = Low		9			9		mA
I_{CCW}	Powered up V_{CC} supply current	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High		140	185		140	185	
	Capacitance	$\overline{CE}_{1,2}$ = High $CE_{3,4}$ = Low							pF
		$V_{CC} = 5.0V$							
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

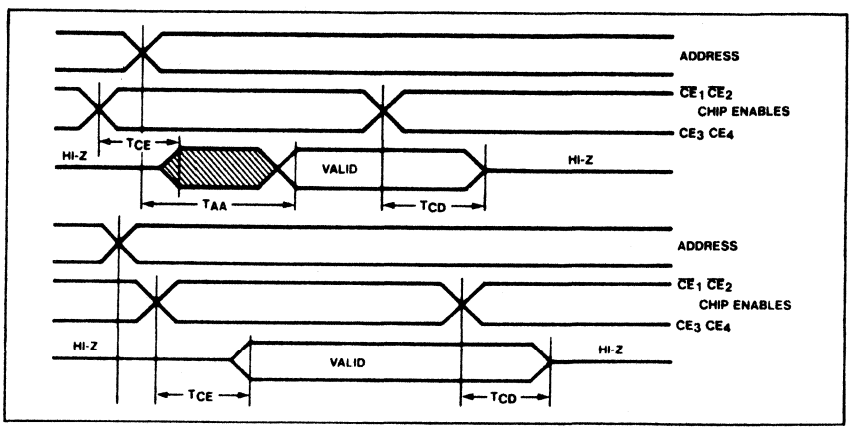
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82PS181: $0°C \le T_A \le +75°C$, $4.75 \le V_{CC} \le 5.25V$
S82PS181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC}$ 5.5V

PARAMETER		TO	FROM	N82PS181			S82PS181			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}		Output	Address		50	70		50	90	
T_{CE}	(Power up access time)[3]	Output	Chip enable			70			90	
	Disable time									ns
T_{CD}		Output	Chip disable		20	40		20	50	

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES

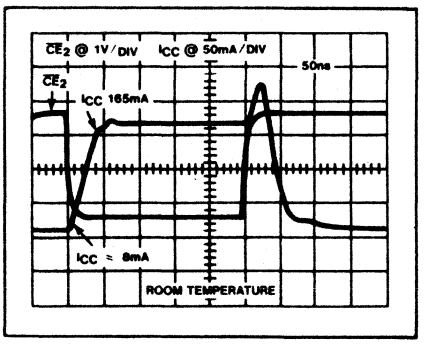
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.
3. Care should be taken to follow stated *power supply and circuit layout considerations.*

POWER SUPPLY AND CIRCUIT LAYOUT CONSIDERATIONS

A device power up sequence is initiated by on-chip circuitry in response to a true chip select assertion. When the memory is deselected, I_{CC} idles at a standby current of I_{CCS}, and then increases to I_{CCP} during power up. Because the transition from standby to full power operation is very rapid (4A/μS), the system power supply must be designed to handle an effective step surge in current equal to I_{CCP}-I_{CCS}; or about 155mA. If this surge is not properly treated, not only in power supply design, but in circuit board layout and device power supply bypassing, glitches on the GND and V_{CC} rails could result. These transients delay the settling of on-chip address decode circuits, which functionally extends the device's power up access time, T_{CE}, beyond that which is specified as maximum.

It is recommended that all printed circuit board traces supplying device V_{CC} and GND levels maximize their trace widths to reduce in-line inductance. Ideally separate power and ground planes should be incorporated into the PCB to not only provide low inductance power supply connections but also to add a high frequency uniform power supply bypass. In addition to this, each device should be bypassed from V_{CC} to GND with 0.1μf high frequency capacitor. Capacitor connections should be made as close to the device's pins as physically possible.

I_{CCW} (MAX) is the maximum steady state current of enabled operation. Upon disable the I_{CC} surges (25ns) to a value which is about 20% above I_{CCW} and then decreases to I_{CCS} with a slew rate of 5A/μS.



(12% Low resistors)

(All outputs are on when enabled)

PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					
V_{CCP}	To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					
V_{CCH}	Upper		5.3	5.5	5.7	V
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					
V_{IH}	High		2.4		5.5	V
V_{IL}	Low		0	0.4	0.8	
	Input current					
I_{IH}	High	V_{IH} = +5.5V			50	μA
I_{IL}	Low	V_{IL} = +0.4V			−500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_p	CE programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	V_{CC} = V_{CCP}			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

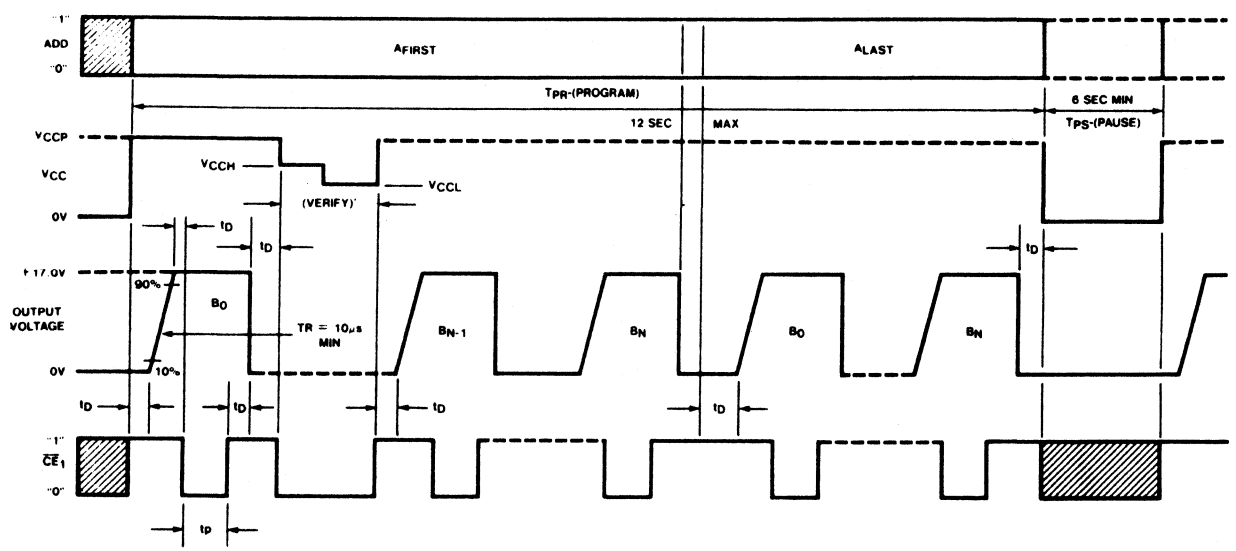
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High, $\overline{CE}_2$ = Low, CE_3 = High and CE_4 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the $\overline{CE}_1$ input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S2708-F,R

DESCRIPTION

The 82S2708 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S2708 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S2708 is available only in the military temperature range. For the military temperature range (-55°C to +125°C) specify S82S2708, F or R.

Pins 21, 19 and 18 have no internal connections, therefore -5V, +12 and programming voltages used by MOS devices will have no effect on this bipolar device.

FEATURES

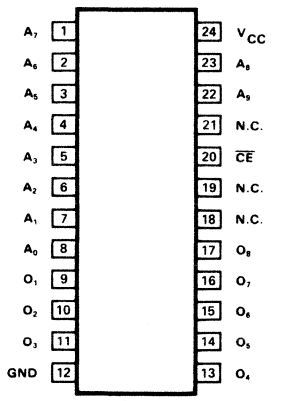
- **Address access time:**
  S82S2708: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  S82S2708: -150μA max
- **Chip enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Pin for pin replacement for 2708 EROM**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

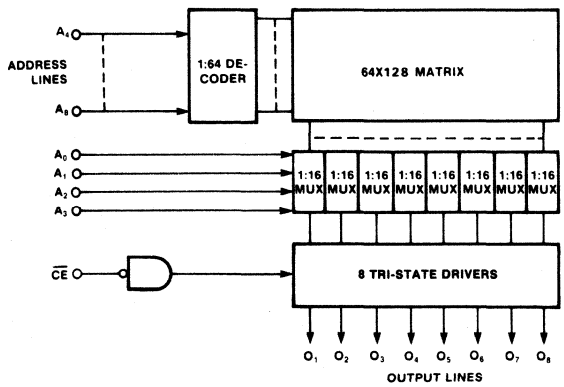
PIN CONFIGURATION

F,R PACKAGE*



*F = Cerdip R = Flat Pak
NC = No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	S82S2708	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	S82S2708			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				80	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2	
	Output voltage	$\overline{CE}$ = Low				V
V_{OL}	Low	I_{OUT} = 9.6mA			0.5	
V_{OH}	High	I_{OUT} = -2.0mA	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-150	
I_{IH}	High	V_{IN} = 5.5V			50	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			60	
I_{OS}	Short circuit	$\overline{CE}$ = Low, V_{OUT} = 0V, Stored High	-15		-85	mA
I_{CC}	V_{CC} supply current				185	mA
	Capacitance	$\overline{CE}$ = High V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF

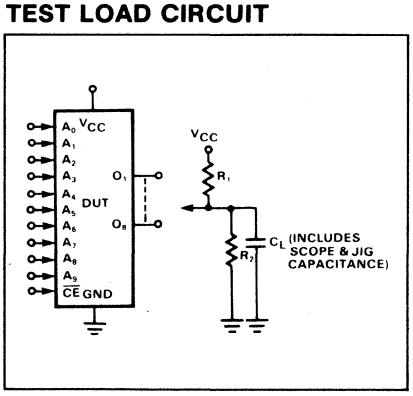
S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	S82S2708			UNIT
				Min	Typ	Max	
	Access time						ns
T_{AA}		Output	Address			90	
T_{CE}		Output	Chip enable			50	
	Disable time						ns
T_{CD}		Output	Chip disable			50	

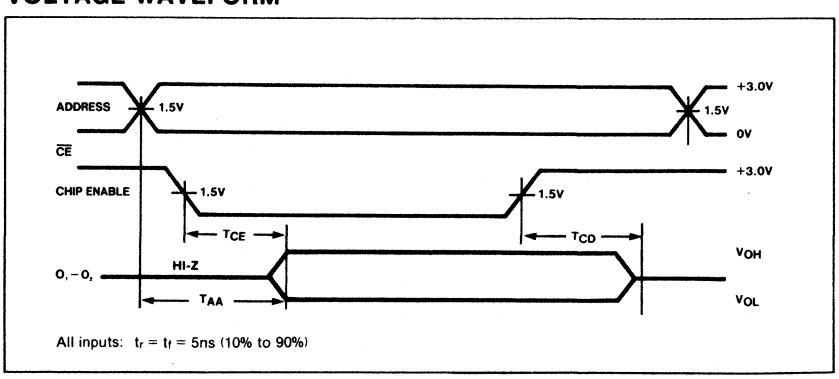
NOTES

1. Positive current is defined as into the terminal referenced.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f$ = 5ns (10% to 90%)

82S183-F,G,N,R

DESCRIPTION

The 82S183 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S183 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the output drivers are controlled solely by $\overline{CE}_1$, $\overline{CE}_2$, and CE_3 lines.

A D-type latch is used to enable the tri-state output drivers. In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

The 82S183 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S183, for F or N, and for the military temperature range (−55°C to 125°C) specify S82S183, F, G or R.

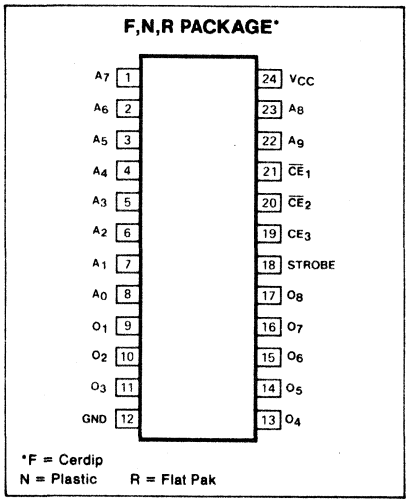
FEATURES

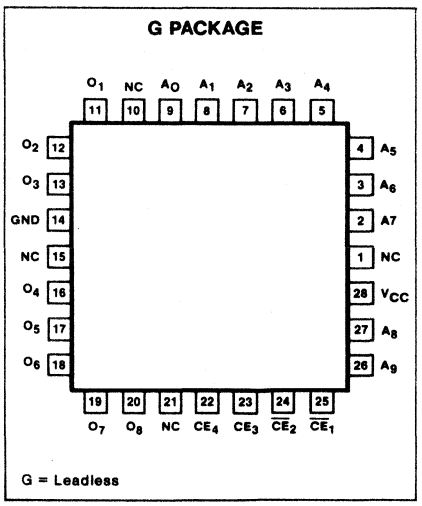
- **Address access time:**
  N82S183: 60ns max
  S82S183: 90ns max
- **Power dissapation: 85μW/bit typ**
- **Input loading:**
  N82S183: −100μA max
  S82S183: −150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

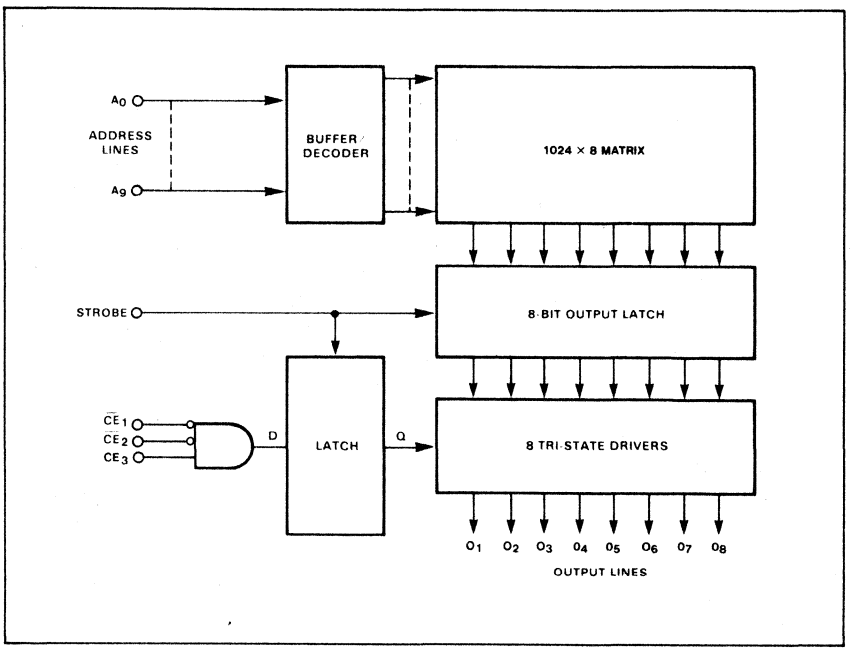
- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S183	0 to +75	
	S82S183	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S183: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S183: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS[4]	N82S183			S82S183			UNIT
			Min	Typ[6]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2			−1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low, CE_3 = Strobe = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = −2.0mA			2.4				
	Input current[4]								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V	25		25			50	
	Output current[4]								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High or CE = Low, V_{OUT} = 5.5V			40			100	μA
		$\overline{CE}$ = High or CE = Low, V_{OUT} = 0.5V			−40			−100	
I_{OS}	Short circuit[1]	$\overline{CE}$ = Low, CE = High, V_{OUT} = 0V, High stored	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current			130	175			185	mA
	Capacitance	$\overline{CE}_{1,2}$ = High or CE_3 = Low, V_{CC} = 5.0							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82S183: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S183: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

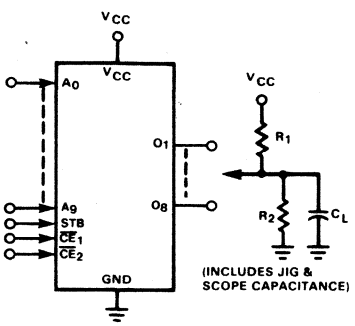
PARAMETER		TO	FROM	TEST CONDITIONS	N82S183			S82S183			UNIT
					Min	Typ[6]	Max	Min	Typ	Max	
	Access time[2]			Latched or transparent read							ns
T_{AA}		Output	Address			45	60			90	
T_{CE}		Output	Chip enable			25	40			50	
T_{CD}	Disable time[2]	Output	Chip disable	Latched or transparent read		25	40			50	ns
	Setup and hold time[3]			Latched read only							ns
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10			10			
T_{ADH}	Hold time	Output	Address		0			5			
	Pulse width[3]			Latched read only							ns
T_{SW}	Strobe				30	15		40			
	Latch time[3]			Latched read only							ns
T_{SL}	Strobe				60	35		90			
	Delatch time[3]			Latched read only							ns
T_{DL}	Strobe						30			35	

NOTES on following page.

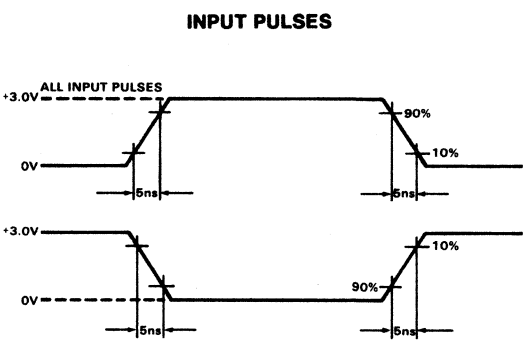
NOTES

1. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
2. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid date will appear T_{AA} nanoseconds after the address has changed the T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
3. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
4. Positive current is defined as into the terminal referenced.
5. Areas shown by crosshatch are latched data from previous address.
6. Typical values are at V_{CC} = 5V, T_A = 25°C

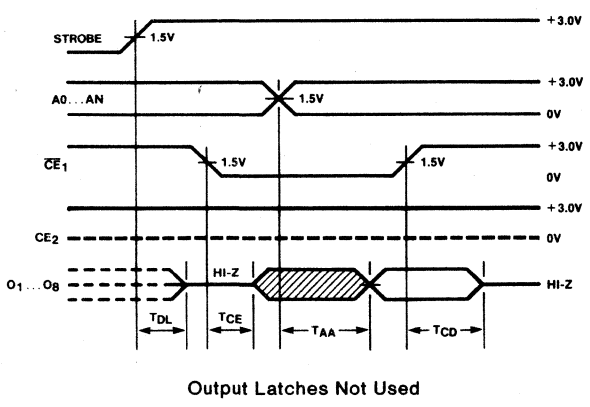
TEST LOAD CIRCUIT



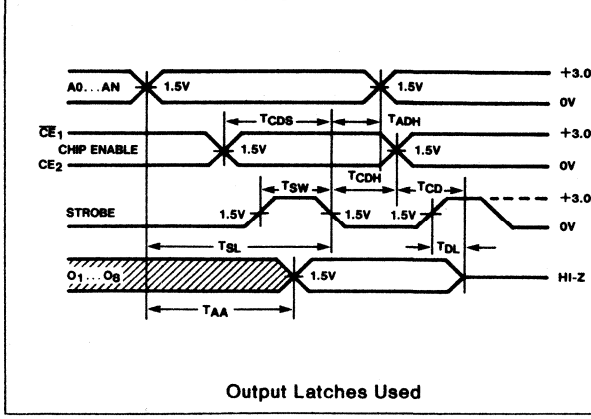
VOLTAGE WAVEFORM



TIMING DIAGRAMS



Output Latches Not Used



Output Latches Used

82S185-I,F,N,R

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S185 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

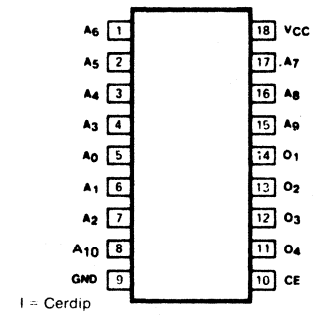
This device includes on-chip decoding and 1 chip enable input for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S185 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S185, I, F, N, and for the military temperature range (–55°C to +125°C) specify S82S185, I, F, or R.

FEATURES

- **Low power dissipation: 50μW/bit typ**
- **Address access time:**
  N82S185: 100ns max
  S82S185: 115ns max
- **Input loading:**
  N82S185: –100μA max
  S82S185: –150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

I,F,N PACKAGE

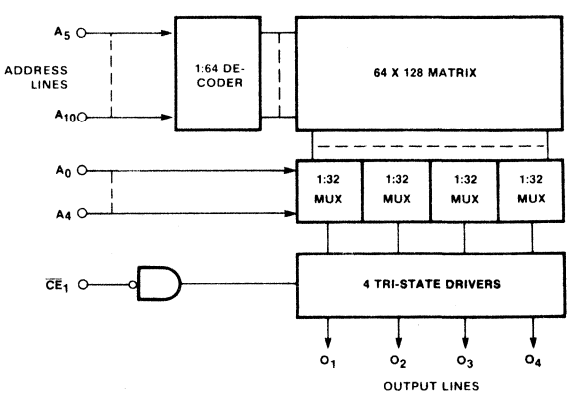


I = Cerdip
F = Cerdip
N = Plastic R = Flat Pak

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S185	0 to +75	
	S82S185	-55 to +125	
T_{STG}	Storage	-65 to +150	

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

N82S185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82S185			S82S185			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage[1]								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage[1]	$\overline{CE}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN}= 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_O (OFF)	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_{OUT} = 0V High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			90	120			130	mA
	Capacitance	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

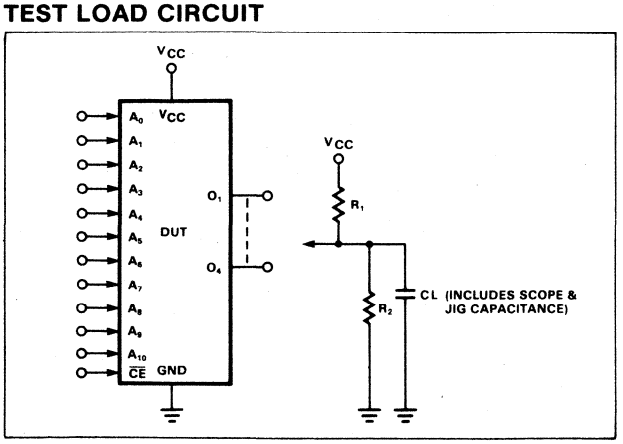
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF
N82S185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S185			S82S185			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[4]	Output	Address		70	100			115	
T_{CE}	Output	Chip enable		30	40			50	
Disable time									ns
T_{CD}	Output	Chip disable		30	40			50	

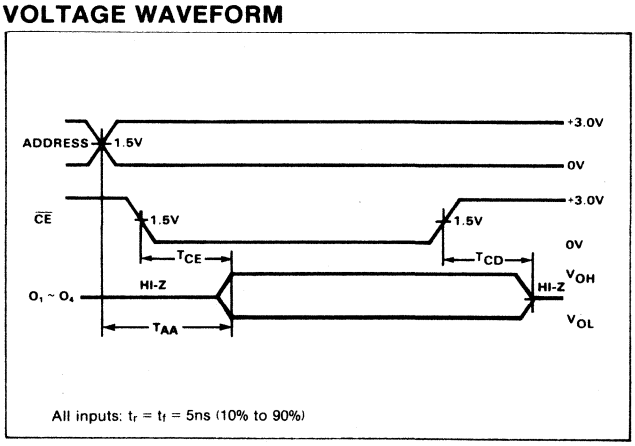
NOTES

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. All typical values are at I_{CC} 50, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PRELIMINARY DATA SHEET 82HS185-I,F,N,R

DESCRIPTION

The 82HS185 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82HS185 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

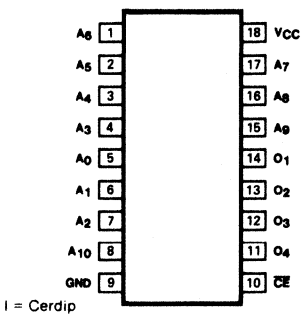
These devices include on-chip decoding and 1 chip enable input for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS185 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82HS185, I, F N, and for the military temperature range (-55°C to +125°C) specify S82HS185, I, F, or R.

FEATURES

- **Low power dissipation: 50μW/bit typ**
- **Address access time:**
  N82HS185: 60ns max
  S82HS185: 80ns max
- **Input loading:**
  N82HS185: -100μA max
  S82HS185: -150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

I,F,N,R PACKAGE

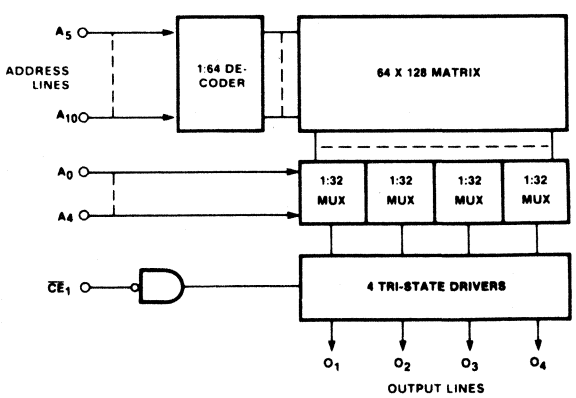


I = Cerdip
F = Cerdip
N = Plastic R = Flat Pak

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82HS185	0 to +75	
	S82HS185	-55 to +125	
T_{STG}	Storage	-65 to +150	

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

N82HS185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82HS185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82HS185			S82HS185			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage[1]								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage[1]	$\overline{CE}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN}= 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_O (OFF)	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_{OUT} = 0V High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			110	155			155	mA
	Capacitance	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

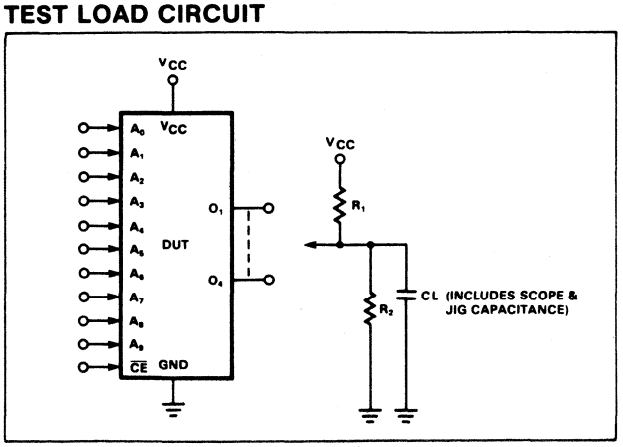
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF
N82HS185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82HS185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S185			S82S185			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[4]	Output	Address		45	60			80	
T_{CE}	Output	Chip enable		20	30			40	
Disable time									ns
T_{CD}	Output	Chip disable		20	30			40	

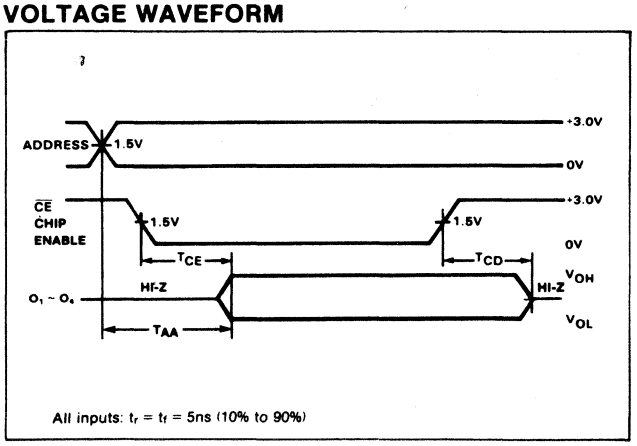
NOTES

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. All typical values are at V_{CC} = 5V, TA = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S191-I,G,N,R

DESCRIPTION

The 82S191 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S191 is supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S191 device is available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82191, I, N, and for the military temperature range (–55°C to +125°C) specify S82S191, I, R or G.

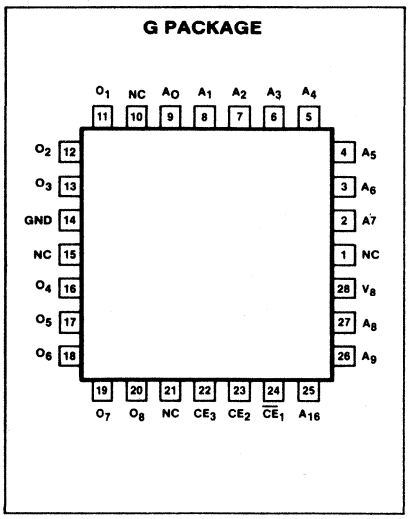
FEATURES

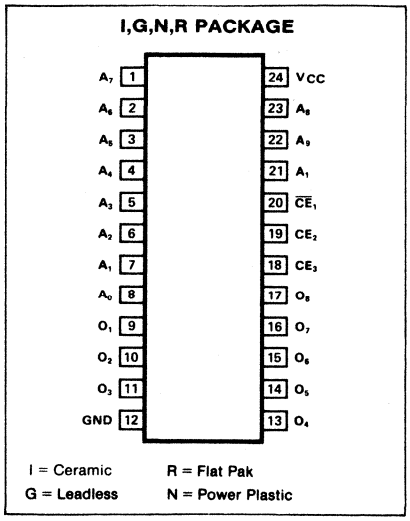
- **Address access time:**
  N82S191: 80ns max
  S82S191: 100ns max
- **Power dissipation : 40μW/bit typ**
- **Input loading:**
  N82S191: -100μA max
  S82S191: -150μA max
- **3 chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

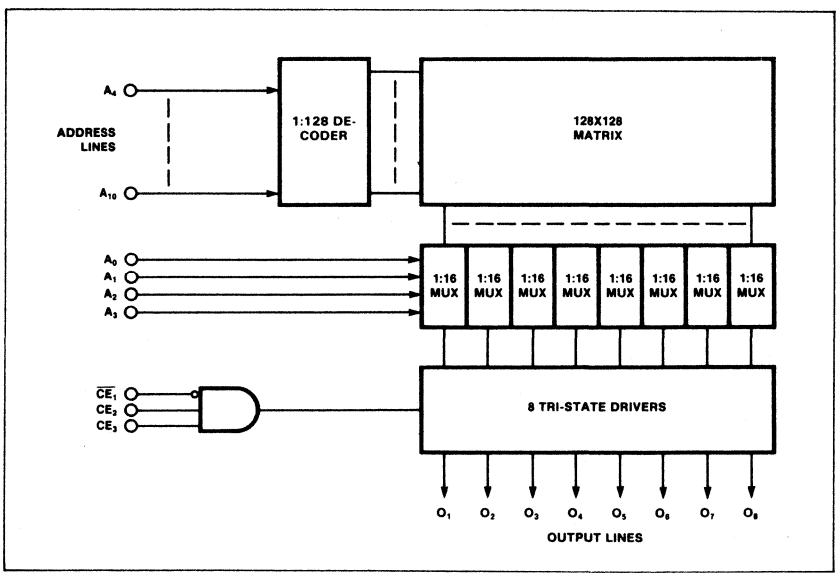
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S191	0 to +75	
	S82S191	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S191: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S191: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S191			S82S191			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								μA
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 0.5			-40			-60	
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 5.5			40			60	
I_{OS}	Short circuit	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175			185	mA
	Capacitance	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

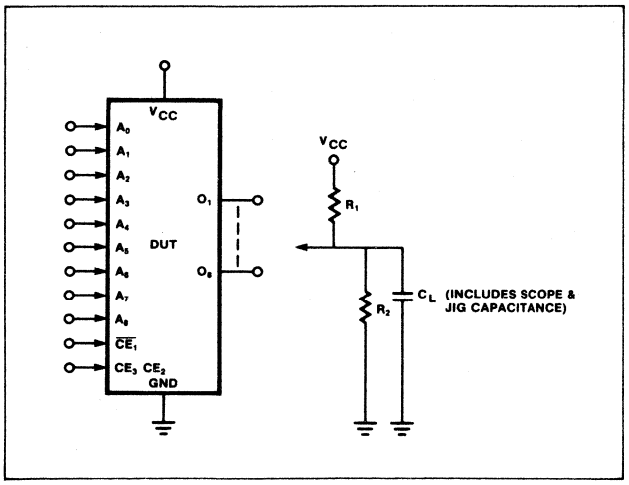
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S191: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S191: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S191			S82S191			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
	Access time								ns
T_{AA}[2]	Output	Address		50	80			100	
T_{CE}	Output	Chip enable		20	40			50	
	Disable time								ns
T_{CD}	Output	Chip disable		20	40			50	

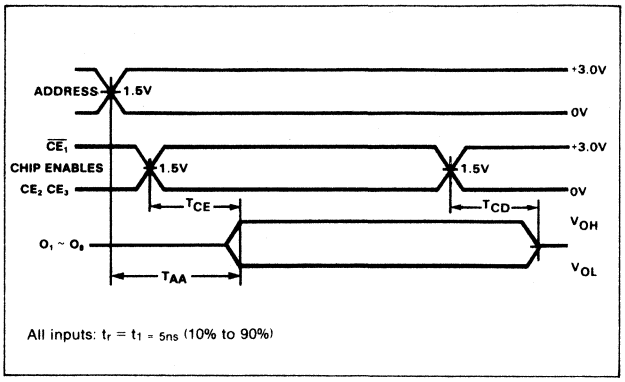
NOTES

1. Positive current is defined as into the terminal referenced.
2. Tested at an address cycle time of 1 μsec.
3. All typical values are at V_{CC} = 50, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

DESCRIPTION

The 82HS191 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82HS191 is supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS191 device is available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82HS191, I, N, and for the military temperature range (-55°C to +125°C) specifiy S82HS191, I, R or G.

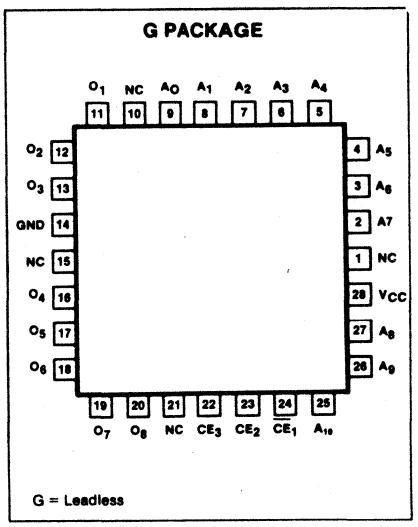
FEATURES

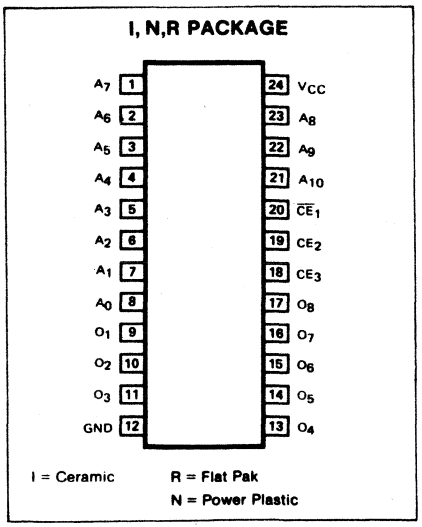
- **Address access time:**
  N82HS191: 60ns max
  S82HS191: 80ns max
- **Power dissipation: 20μW/bit typ**
- **Input loading:**
  N82HS191: -100μA max
  S82HS191: -150μA max
- **3 chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

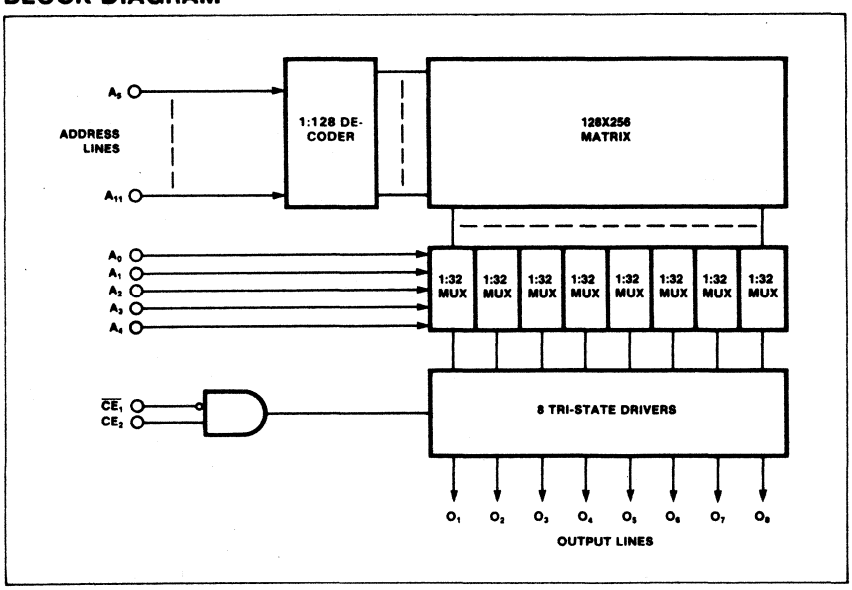
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82HS191	0 to +75	
	S82HS191	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82HS191: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

S82HS191: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82HS191			S82HS191			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								μA
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 0.5			-40			-60	
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 5.5			40			60	
I_{OS}	Short circuit	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175			185	mA
	Capacitance	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82HS191: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

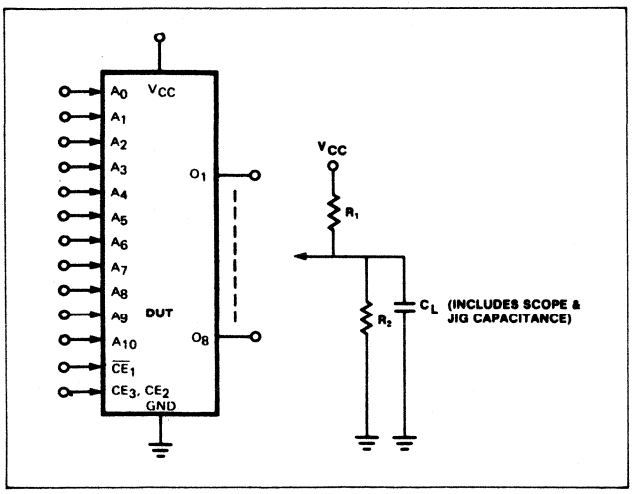
S82HS191: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82HS191			S82HS191			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[2]	Output	Address		50	60			80	
T_{CE}	Output	Chip enable		20	35			45	
Disable time									ns
T_{CD}	Output	Chip disable		20	35			45	

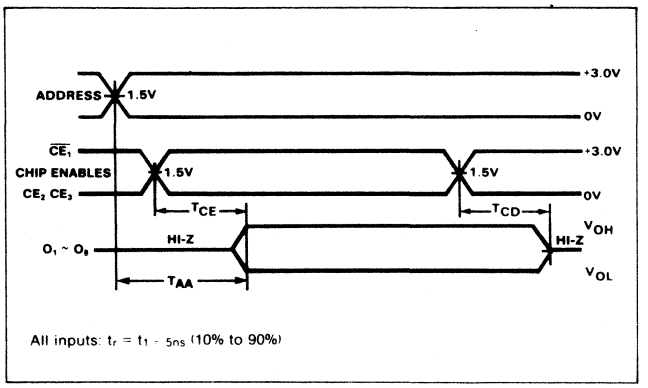
NOTES

1. Positive current is defined as into the terminal referenced.
2. Tested at an address cycle time of 1 μsec.
3. All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (Fp), or true active-low ($\overline{F}_P$). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101, F or N, and for the military temperature range (-55°C to +125° C) specify S82S100/101, F or G, I, R.

LOGIC FUNCTION

Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions: @ $\overline{CE} = 0$:
$F_0 = (P_0 + P_1 + P_2)$ @ L = Closed
$F_0 = (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ L = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $\overline{F}_P$ (active low) is available, but not both. The required function polarity is programmed via link (L).

FEATURES

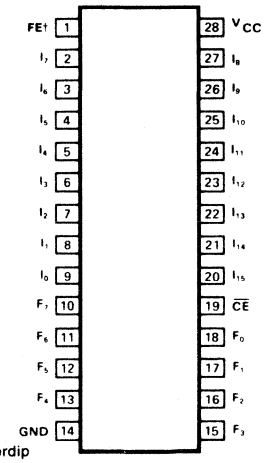
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **Address access time:**
  S82S100/101—80ns Max
  N82S100/101—50ns Max
- **Power dissipation: 600mW typ**
- **Input loading:**
  S82S100/101: −150μA Max
  N82S100/101: −100μA Max
- **Chip enable input**
- **Output option:**
  82S100: Tri-state
  82S101: Open collector
- **Output disable function:**
  Tri-state—Hi-Z
  Open collector—Hi

APPLICATIONS

- CRT display systems
- Random logic
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Sequential controllers
- Data security encoders
- Fault detectors
- Frequency synthesizers

PIN CONFIGURATION

F,G,I,N,R PACKAGE*

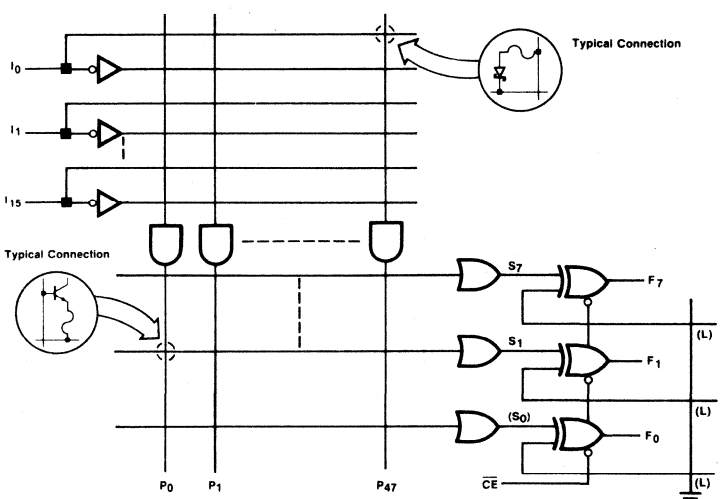


*F = Cerdip
G = Leadless I = Ceramic N = Plastic R = Flat pak
†Open or grounded during normal operation

TRUTH TABLE

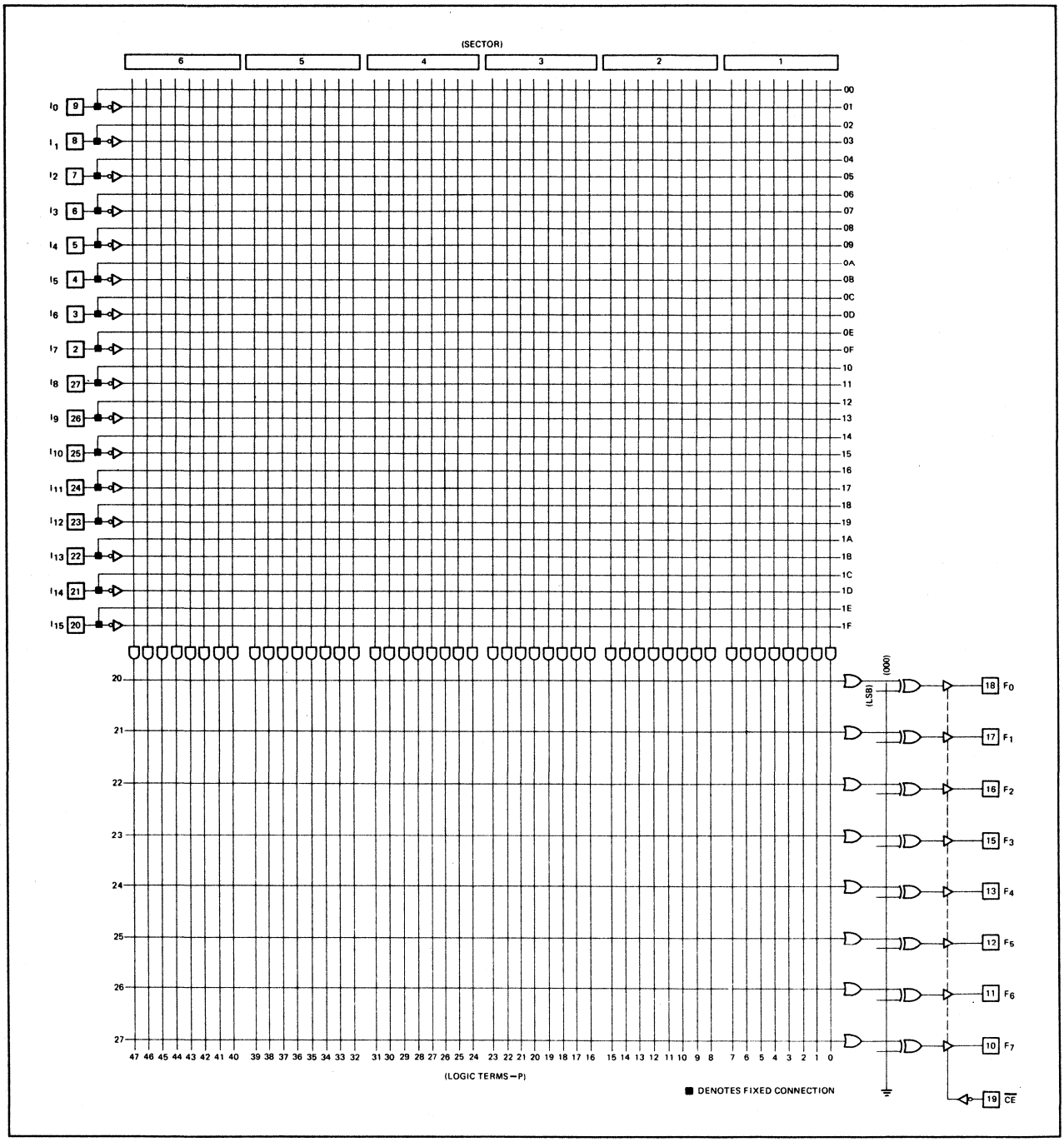
MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	$\overline{F}_p$
Disabled (82S101)	X	1	X	1	1
Disabled (82S100)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

LOGIC DIAGRAM



Notes
1. Fusible Ni-Cr links exist initially intact at all array cross-points.
2. ■ = fixed connection.

FPLA LOGIC DIAGRAM



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	-55	+125	
T_{STG}	Storage	-65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S100/101: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	**High**	V_{CC} = Max	2			2			
V_{IL}	**Low**	V_{CC} = Min			0.85			0.8	
V_{IC}	**Clamp[3,4]**	V_{CC} = Min, I_{IN} = -18mA		**-0.8**	-1.2		**-0.8**	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	**High (82S100)[3,5]**	I_{OH} = -2mA	2.4			2.4			
V_{OL}	**Low[3,6]**	I_{OL} = 9.6mA		**0.35**	0.45		**0.35**	0.50	
	Input current								µA
I_{IH}	High	V_{IN} = 5.5V		**<1**	25		**<1**	50	
I_{IL}	Low	V_{IN} = 0.45V		**-10**	-100		**-10**	-150	
	Output current	$\overline{CE}$ = High, V_{CC} = Max							
I_{OLK}	**Leakage[7]**	V_{OUT} = 5.5V		**1**	40		**1**	60	µA
$I_{O(OFF)}$	**Hi-Z state (82S100)[7]**	V_{OUT} = 5.5V		**1**	40		**1**	60	µA
		V_{OUT} = 0.45V		**-1**	-40		**-1**	-60	
I_{OS}	**Short circuit (82S100)[4,8]**	$\overline{CE}$ = Low, V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	**V_{CC} supply current[9]**	V_{CC} = Max		**120**	170		**120**	180	mA
	Capacitance[7]	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Access time									ns
T_{IA}	Input	Output	Input		**35**	50		**35**	**80**	
T_{CE}	Chip enable	Output	Chip enable		**15**	30		**15**	**50**	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		**15**	30		**15**	**50**	

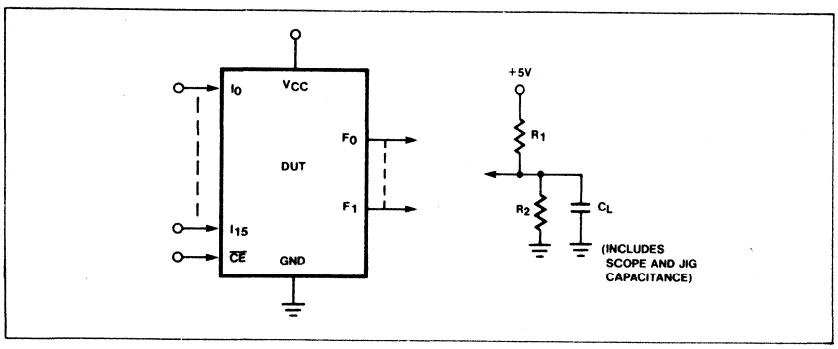
NOTES on following page.

OBJECTIVE SPECIFICATION

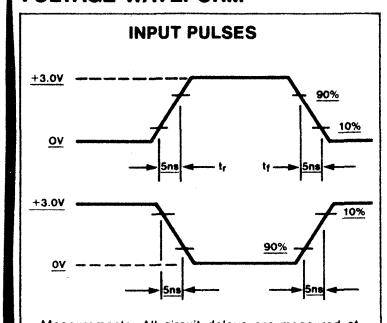
INTEGRATED FUSE LOGIC
SERIES 28

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation of the device specifications is not implied.
2. All voltage values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

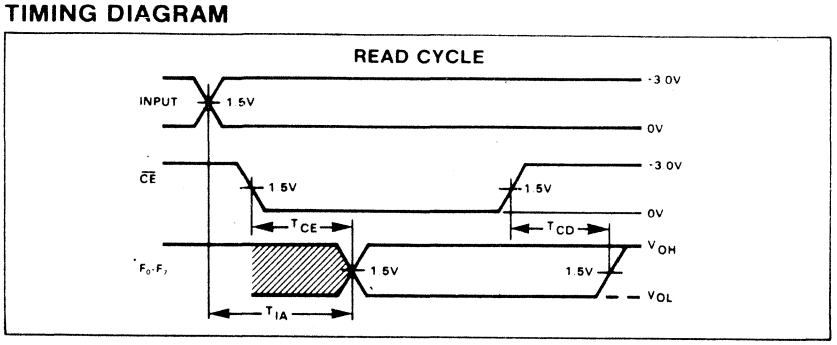


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

VIRGIN DEVICE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "false").
3. The "OR" Matrix contains all 48-P-terms.
4. The polarity of each output is set to active high (F_P function).
5. All outputs are at a low logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the "AND" matrix, "OR" matrix, and output polarity outlined below. To maximize recovery from programming errors, leave all links in unused device areas intact.

SET-UP

Terminate all device outputs with a 10K resistor to +5V. Set GND (pin 14) to 0V.

Output Polarity

PROGRAM ACTIVE LOW ($\overline{F_P}$ FUNCTION)

Program output polarity before programing "AND" matrix and "OR" matrix. Program 1 output at the time. (L) links of unused outputs are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Set V_{CC} (pin 28) to V_{CCL}.
3. Set $\overline{CE}$ (pin 19), and I_0 through I_{15} to V_{IH}.
4. Apply V_{OPH} to the appropriate output, and remove after a period t_p.
5. Repeat step 4 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCS}.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Address a non-existent P-term by applying V_{IH} to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a high logic level are programmed active low (F_P function), while all outputs at a low logic level are programmed active high ($\overline{F_P}$ function).
5. Return V_{CC} to V_{CCP} or V_{CCL}.

"AND" Matrix

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set FE (pin 1) to V_{FEL}, and V_{CC} (pin 28) to V_{CCP}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.
5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.
5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step 6.
5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step 6.
6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.
6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_P.
6c. After t_D delay, return FE input to V_{FEL}.
7. Disable programmed input by returning I_0 to V_{IX}.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCP}.
2. Enable F_7 output by setting $\overline{CE}$ to V_{IX}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.
5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage at I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.
   B. Lower the input voltage at I_0 from V_{IH} to V_{IL}, and sense the logic state output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	INPUT VARIABLE STATE CONTAINED IN P-TERM
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Don't Care
0 1	0 0	(I_0), $(\overline{I_0})$

Note that 2 tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Disable verified input by returning I_0 to V_{IX}.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{IX} from all input variables.

"OR" MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links in the "OR" matrix corresponding to unused outputs and unused P-terms are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_6 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB.
5a. If the P-term is contained in output function F_0 ($F_0 = 1$ or $\overline{F_0} = 0$), got to step 6, (fusing cycle not required).
5b. If the P-term is **not** contained in output function F_0 ($F_0 = 0$ or $\overline{F_0} = 1$), set to fuse the P_n link by forcing output F_0 to V_{OPF}.
6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.
6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_P.
6c. After t_D delay, return FE input to V_{FEL}.
6d. After t_D delay, remove V_{OPF} from output F_0.
7. Repeat steps 5 and 6 for all other output functions.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{CCS} from V_{CC}.

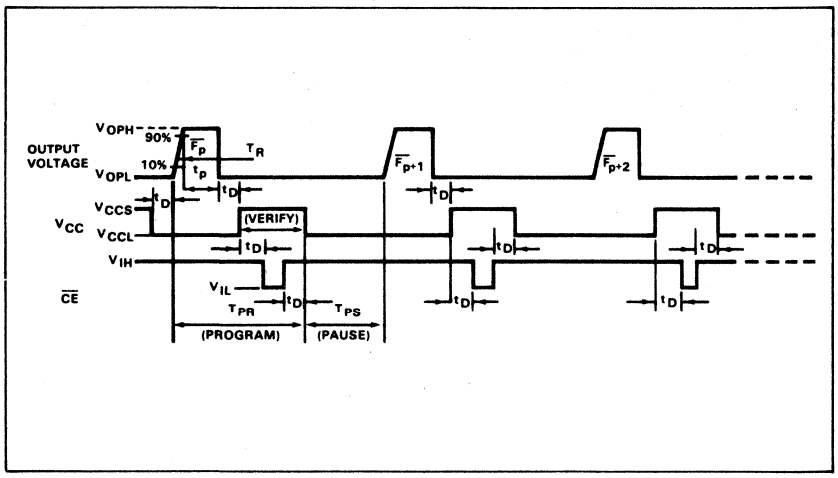
VERIFY PRODUCT TERM

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_0 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.
5. After t_D delay, enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
6. To determine the status of the P_n link in the "OR" matrix for each output function F_p or $\overline{F_p}$, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

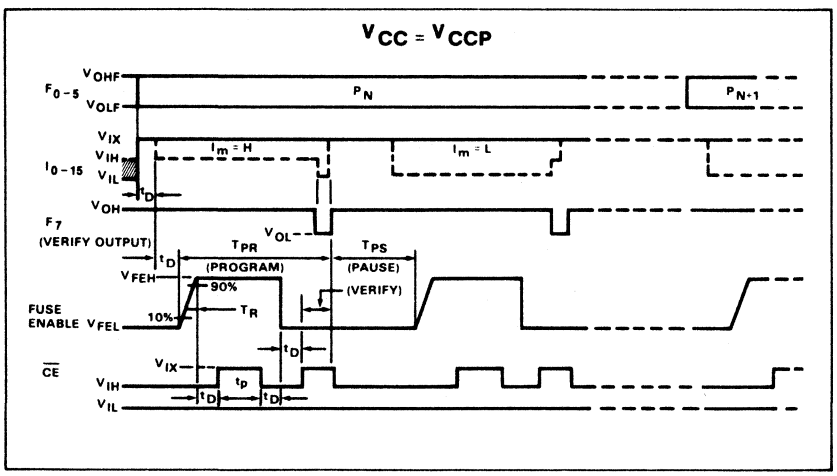
OUTPUT		P-TERM LINK
Active High (F_p)	Active Low ($\overline{F_p}$)	
0 1	1 0	**Fused** **Present**

7. Repeat steps 4 through 6 for all other P-terms.
8. Remove V_{CCS} from V_{CC}.

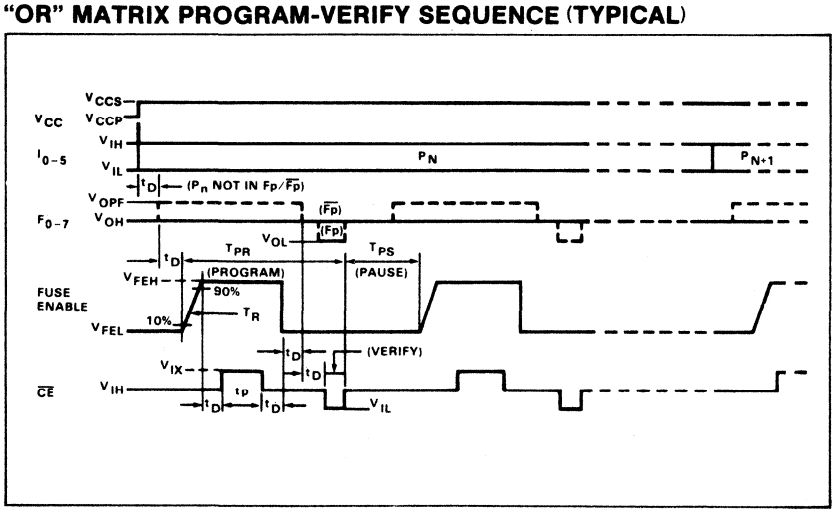
OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



"AND" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



"OR" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



PROGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCS}	V_{CC} supply (program/verify "OR", verify output polarity)[2]	I_{CCS} = 550mA, min. Transient or steady state	8.25	8.5	8.75	V
V_{CCL}	V_{CC} supply (program output polarity)		0	0.4	0.8	V
I_{CCS}	I_{CC} limit (program "OR")	V_{CCS} = +8.5 ± .25V	550		1,000	mA
	Output voltage					V
V_{OPH}	Program output polarity[3]	I_{OPH} = 300 ± 25mA	16.0	17.0	18.0	
V_{OPL}	Idle		0	0.4	0.8	
I_{OPH}	Output current limit (Program output polarity)	V_{OPH} = +17 ± 1V	275	300	325	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
	Forced output voltage					V
V_{OHF}	High		2.4		5.5	
V_{OLF}	Low		0	0.4	0.8	
	Output current					
I_{OHF}	High	V_{OHF} = +5.5V			100	μA
I_{OLF}	Low	V_{OLF} = 0V			-1	mA
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			10	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			10	mA
V_{FEH}	FE supply (program)[3]	I_{FEH} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
V_{FEL}	FE supply (idle)	I_{FEL} = -1mA, max	1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = +17 ± 1V	275	300	325	mA
V_{CCP}	V_{CC} supply (program/verify "AND")	I_{CCP} = 550mA, min. Transient or steady state	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit (program "AND")	V_{CCP} = +5.0 ± .25V	550		1,000	mA
V_{OPF}	Forced output (program)		9.5	10	10.5	V
I_{OPF}	Output current (program)				10	mA
T_R	Output pulse rise time	10% to 90%	10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms[5]
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

1. These are specifications which a Programming System must satisy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μf capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of the FPLA output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
5. These are new limits resulting from device improvements, and which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

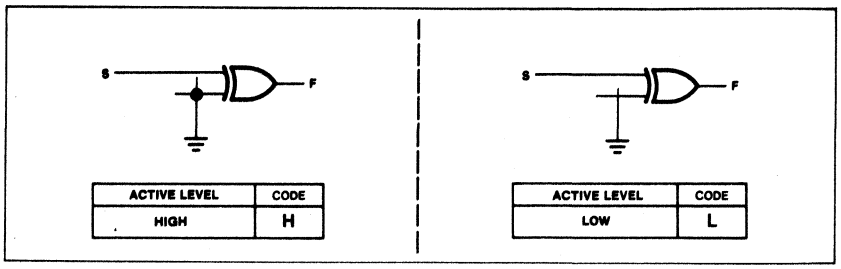
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this Table the logic state or action of variables I, P, and F, associated with each Sum Term S_r, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

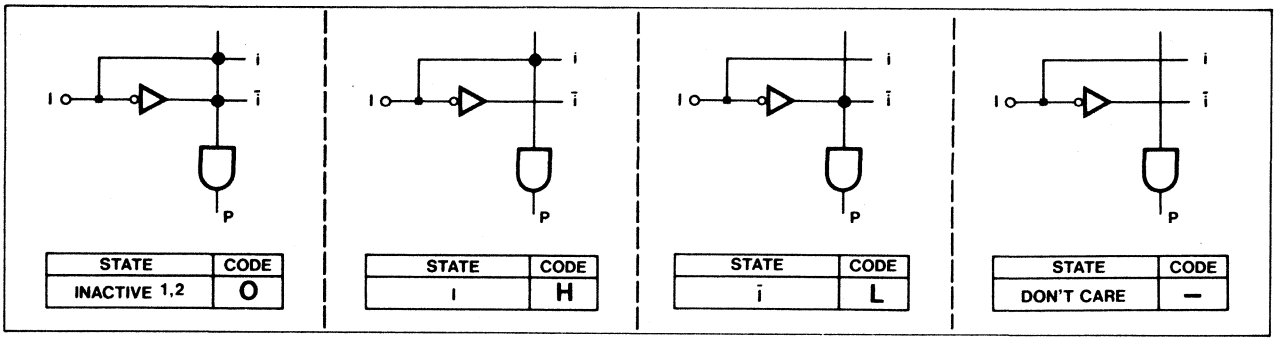
EX-OR ARRAY-(F)



ACTIVE LEVEL	CODE
HIGH	H

ACTIVE LEVEL	CODE
LOW	L

"AND" ARRAY - (I)



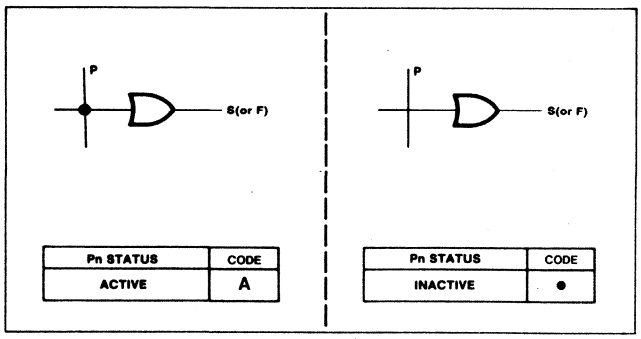
STATE	CODE
INACTIVE [1,2]	O

STATE	CODE
I	H

STATE	CODE
ī	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY - (F)



Pn STATUS	CODE
ACTIVE	A

Pn STATUS	CODE
INACTIVE	•

NOTES

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

FPLA PROGRAM TABLE (Logic)

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____

REV _____ DATE _____

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in Fp	Prod. Term Not Present in Fp	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L

NOTE
Enter (–) for unused inputs of used P-terms

NOTES
1 Entries independent of output polarity
2 Enter (A) for unused outputs of used P-terms

NOTES
1 Polarity programmed once only
2 Enter (H) for all unused outputs

	PRODUCT TERM[1]															
	INPUT VARIABLE[1]															
NO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																
1																
2																
3																
4																
5																
6																
7																
8																
9																
10																
11																
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44																
45																
46																
47																

ACTIVE LEVEL[1]							
OUTPUT FUNCTION[1]							
7	6	5	4	3	2	1	0

(1) Input and Output fields of unused P-terms can be left blank. Unused inputs and outputs are FPLA terminals left floating.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

FPLA PROGRAM TABLE (Memory) 1,2

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV _____ DATE _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	VAR[3,4]
:	600	:	500	:	400	:	300	:	200	:	100	I_0
:	601	:	501	:	401	:	301	:	201	:	101	
:	602	:	502	:	402	:	302	:	202	:	102	I_1
:	603	:	503	:	403	:	303	:	203	:	103	
:	604	:	504	:	404	:	304	:	204	:	104	I_2
:	605	:	505	:	405	:	305	:	205	:	105	
:	606	:	506	:	406	:	306	:	206	:	106	I_3
:	607	:	507	:	407	:	307	:	207	:	107	
:	608	:	508	:	408	:	308	:	208	:	108	I_4
:	609	:	509	:	409	:	309	:	209	:	109	
:	60A	:	50A	:	40A	:	30A	:	20A	:	10A	I_5
:	60B	:	50B	:	40B	:	30B	:	20B	:	10B	
:	60C	:	50C	:	40C	:	30C	:	20C	:	10C	I_6
:	60D	:	50D	:	40D	:	30D	:	20D	:	10D	
:	60E	:	50E	:	40E	:	30E	:	20E	:	10E	I_7
:	60F	:	50F	:	40F	:	30F	:	20F	:	10F	
:	610	:	510	:	410	:	310	:	210	:	110	I_8
:	611	:	511	:	411	:	311	:	211	:	111	
:	612	:	512	:	412	:	312	:	212	:	112	I_9
:	613	:	513	:	413	:	313	:	213	:	113	
:	614	:	514	:	414	:	314	:	214	:	114	I_{10}
:	615	:	515	:	415	:	315	:	215	:	115	
:	616	:	516	:	416	:	316	:	216	:	116	I_{11}
:	617	:	517	:	417	:	317	:	217	:	117	
:	618	:	518	:	418	:	318	:	218	:	118	I_{12}
:	619	:	519	:	419	:	319	:	219	:	119	
:	61A	:	51A	:	41A	:	31A	:	21A	:	11A	I_{13}
:	61B	:	51B	:	41B	:	31B	:	21B	:	11B	
:	61C	:	51C	:	41C	:	31C	:	21C	:	11C	I_{14}
:	61D	:	51D	:	41D	:	31D	:	21D	:	11D	
:	61E	:	51E	:	41E	:	31E	:	21E	:	11E	I_{15}
:	61F	:	51F	:	41F	:	31F	:	21F	:	11F	
:	620	:	520	:	420	:	320	:	220	:	120	F_0
:	621	:	521	:	421	:	321	:	221	:	121	F_1
:	622	:	522	:	422	:	322	:	222	:	122	F_2
:	623	:	523	:	423	:	323	:	223	:	123	F_3
:	624	:	524	:	424	:	324	:	224	:	124	F_4
:	625	:	525	:	425	:	325	:	225	:	125	F_5
:	626	:	526	:	426	:	326	:	226	:	126	F_6
:	627	:	527	:	427	:	327	:	227	:	127	F_7

NOTES:

1. All HEX addresses denote programmable links at Row-Sector locations as shown on the FPLA logic diagram. Sector data specifies the programmed state of fusible links coupling the indicated variable to designated sets of gates. These are sectioned from left to right in HIGH and LOW groups of 4, to which HEX data is assigned in accordance with the definitions below. The LOW group corresponds to least significant HEX digit.
2. Since memory programmers display a continuous address field, 7 "empty" address fields exist between program table sectors, such as (001-OFF), (128-1FF), (228-2FF), etc. The only entry allowed in these fields is "00".
3. Even row addresses in the AND array correspond to links i.
4. Odd row addresses in the AND array correspond to links $\bar{i}$.

SECTOR DATA	ADDRESS	ACTIVE LEVEL
:	000	

TYPICAL TABLE ENTRY

SECTOR DATA	ADDRESS	VAR
5 A	1 00	I_0

PROGRAMMED VARIABLE.

ROW ADDRESS. (00) SELECTS VARIABLE I_0.

SECTOR ADDRESS. (1) SELECTS TERMS 7-0.

(LSD)

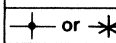
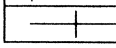
HEX CHARACTER DENOTING PROGRAMMED CONNECTIONS FROM I_0 TO TERMS 3-0.

HEX CHARACTER DENOTING PROGRAMMED CONNECTIONS FROM I_0 TO TERMS 7-4.

MEMORY PROGRAMMING

The FPLA can also be programmed with Memory programming equipment, in conjunction with the FPLA logic diagram. With Memory programming, all links at the AND, OR, and EX-OR array cross-points are treated as memory locations with row-sector addresses. Rows are consecutively scanned while each sector addresses eight Product Terms P_n simultaneously. All necessary gate connections are first translated from the logic equations as "dot" connections at appropriate locations on the logic diagram. The "dot" connection pattern is then transferred to the corresponding Variable-Address locations on the Program Table using (0) = "dot", (1) = blank in a HEX format:

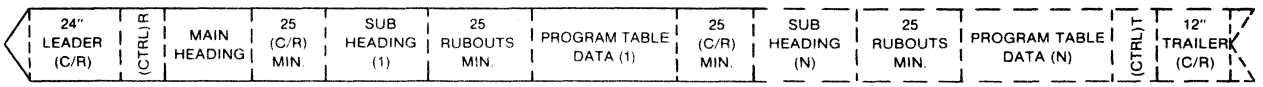
PROGRAMMING DEFINITIONS

LINK	STATUS	CODE
	CLOSED	0
	OPEN	1

TWX TAPE CODING

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



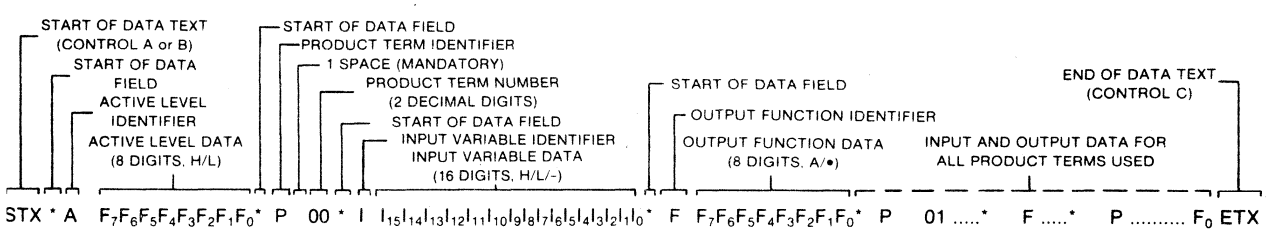
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks in Logic format are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following sequence:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m	$\overline{I_m}$	Don't Care
H	L	— (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp	Product term not present in Fp
A	• (period)

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high	Active low
H	L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

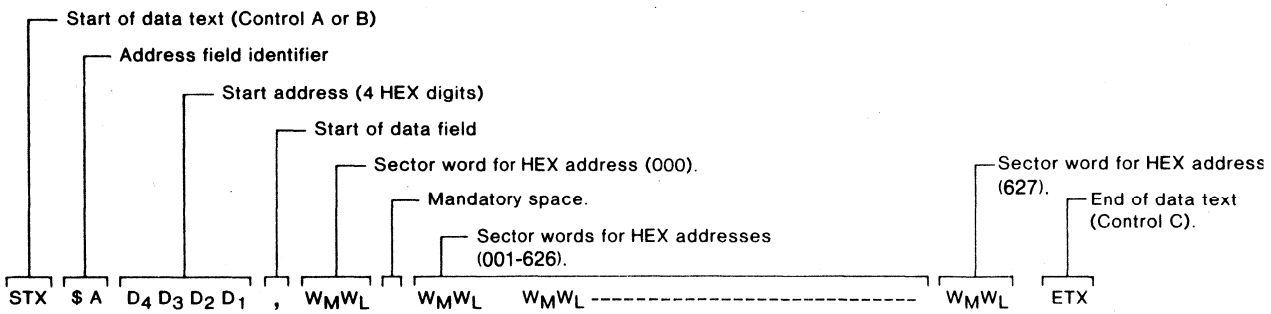
NOTES

1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk(*).
4. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

D. Program Table data blocks in MEMORY format are initiated with an STX character, and terminated with an ETX character.

Carriage return and line feed can be interspersed to achieve any preferred teletype printout from tape.

The body of the data consists of address/data information in accordance with the following ASCII-HEX (Space) format. Address field delimiters may be used to skip over "empty" sector areas:

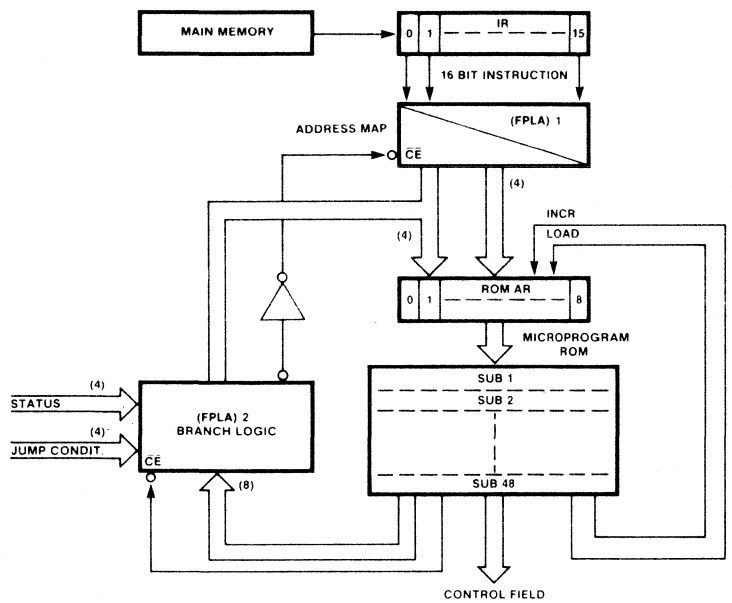


Entries in the data field are made in groups of 8 bits. These are specified with hexadecimal characters $W_M W_L$ followed by a space to separate sequential address entries. In each 8-bit word W_M specifies the most significant 4 bits and W_L designates the least significant 4 bits.

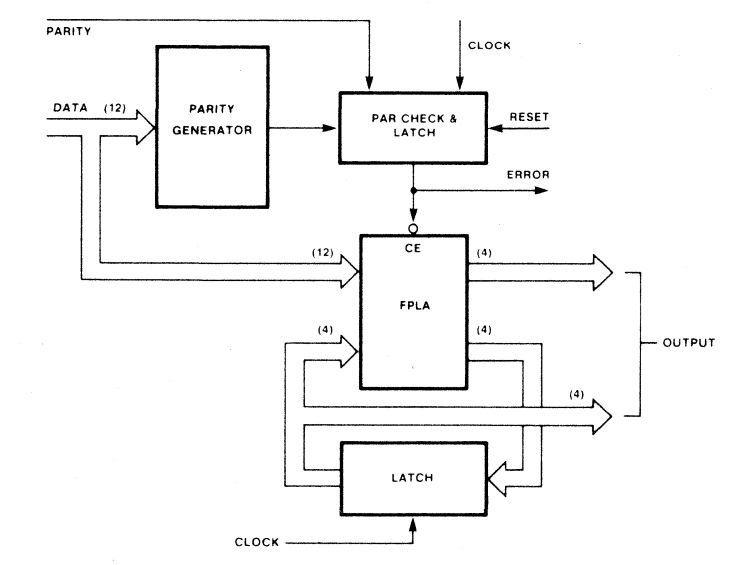
Other ASCII-HEX formats (Percent, Apostrophe, Comma, etc.) are also acceptable. To insure compatibility with other formats consult Signetics or your programmer manual.

TYPICAL APPLICATIONS

SUBROUTINE ADDRESS MAP



SEQUENTIAL CONTROLLER



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S102 and 82S103 are Bipolar programmable AND/NAND gate array, containing 9 gates sharing 16 common inputs. On-chip input buffers enable the user to individually program for each gate either the True (I_m), Complement ($\overline{I_m}$), or Don't Care (X) logic state of each input. In addition, the polarity of each gate output is individually programmable to implement either AND or NAND logic functions.

Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its input variables, and output (DeMorgan theorem).

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, F or N, and for the military range (−55°C to +125°C) specify S82S102/103, F, G, I, and R.

FEATURES

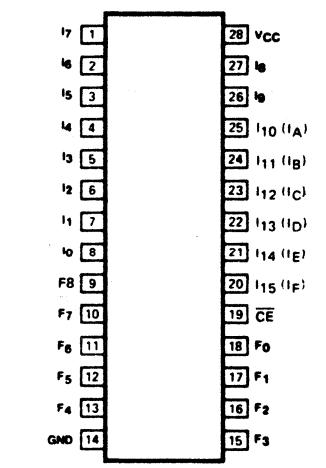
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  N82S102/103: 35ns max
  S82S102/103: 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  N82S102/103: −100μA max
  S82S102/103: −150μA max
- **Output options:**
  82S102: Open collector
  82S103: Tri-state
- **Output disable function:**
  82S102: Hi
  82S103: Hi-Z
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION

F,G,I,N,R PACKAGE*



*F = Cerdip
G = Leadless
I = Ceramic
N = Plastic
R = Flat pack

LOGIC FUNCTION

Typical Output Functions @ $\overline{CE}$ = 0:

At L = Open:

$F_0 = (I_0 \bullet I_1 \bullet I_2 \bullet \ldots . I_m)$

At L = Closed:

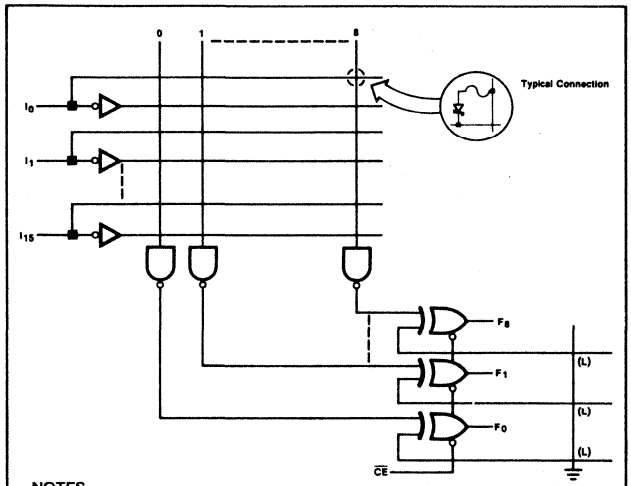
$F_0 = \overline{(I_0 + I_1 + I_2 + \ldots . I_m)}$

m = 0, 1, 2, ... 15

NOTES

For each of the 9 outputs, either the function Fp (active high) or $\overline{Fp}$ (active low) is available but not both. The required function polarity is programmed via link (L).

LOGIC DIAGRAM

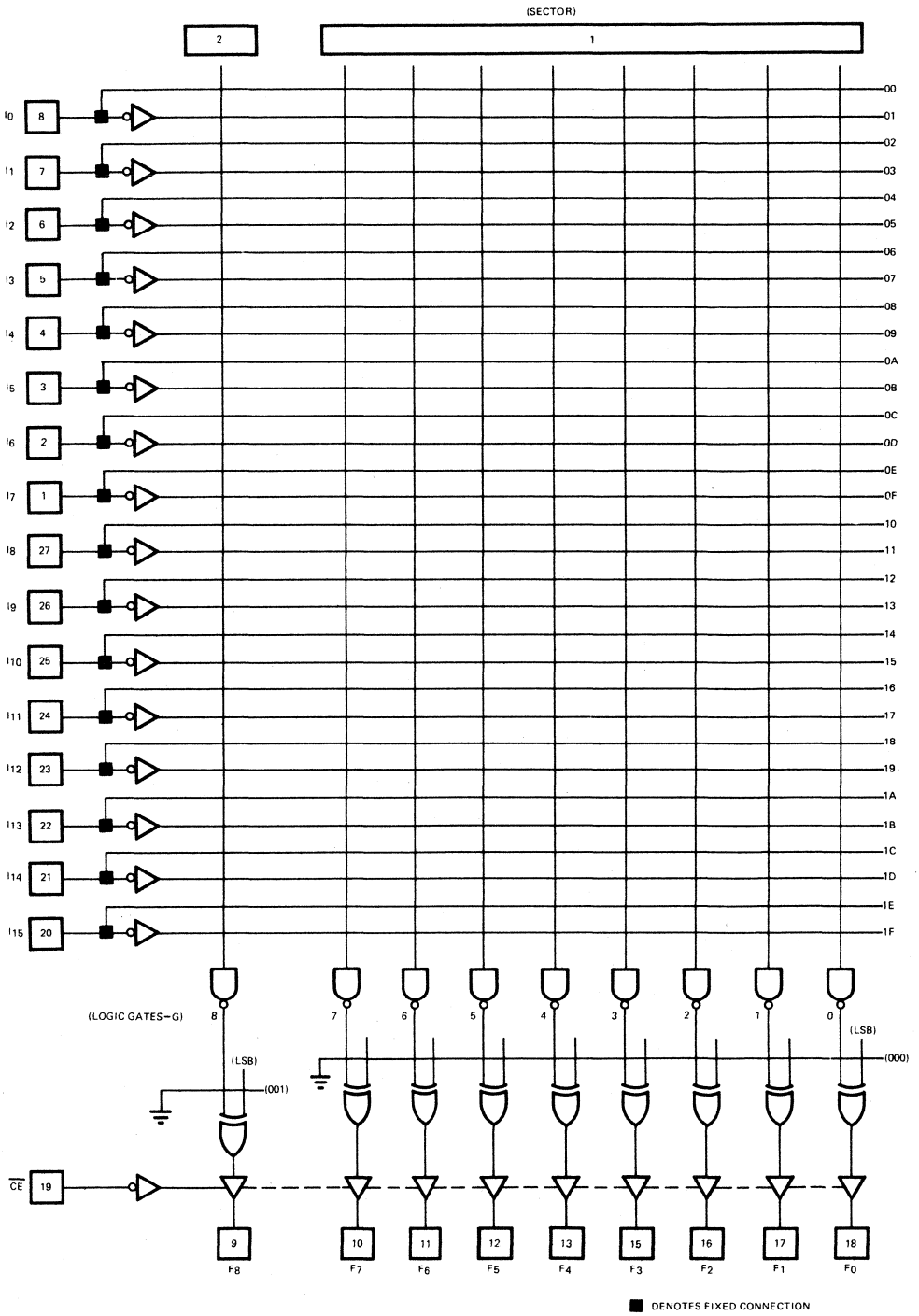


NOTES
1. Fusible Ni-Cr links exist initially intact at all array cross-points.
2. ■ = fixed connection.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	−55 to +125	
T_{STG}	Storage	−65 to +150	

FPGA LOGIC DIAGRAM



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

DC ELECTRICAL CHARACTERISTICS

N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

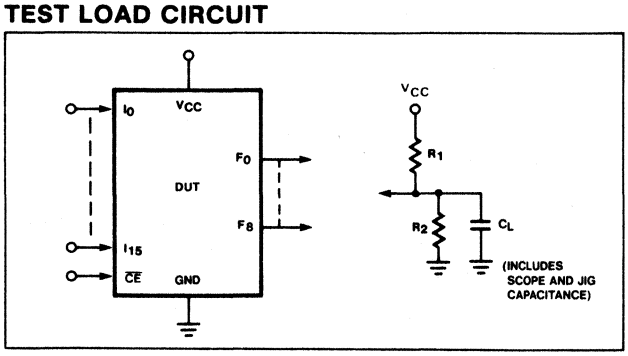
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S102/103			S82S103/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		20	35		20	55	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	45	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	45	

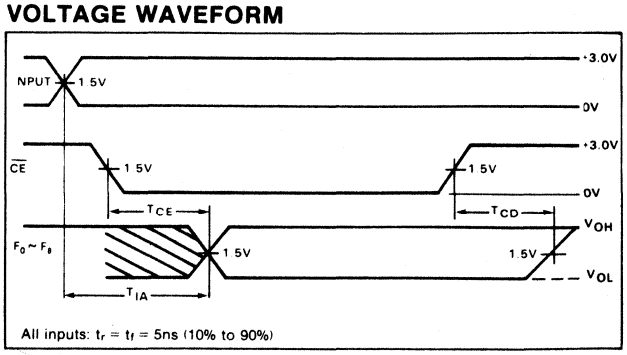
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

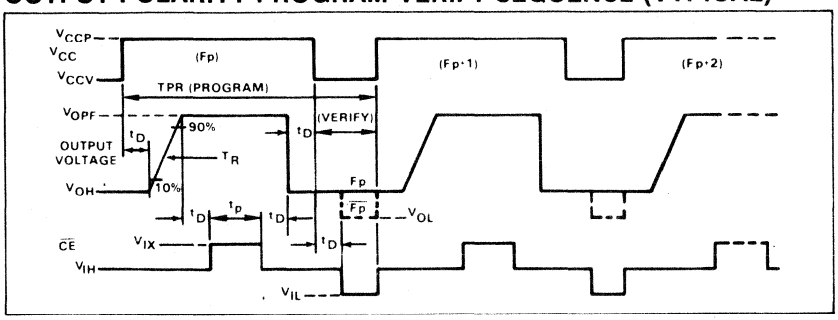
TEST LOAD CIRCUIT



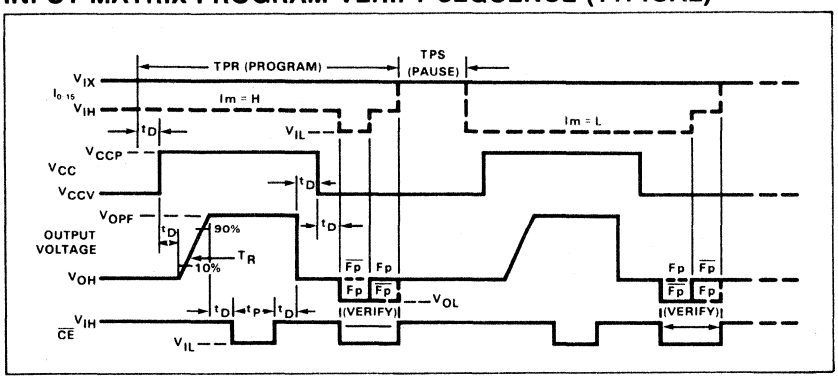
VOLTAGE WAVEFORM



OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



INPUT MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



VIRGIN DEVICE

The 82S102/103 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each gate contains both true and complement values of every input variable I_m (logic Null state).
3. The polarity of each output is set to active low ($\overline{Fp}$ function).
4. All outputs are at a high logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 9 Boolean logic functions of 16 True, Complement, or Don't Care input variables follow the program/verify procedures for the Input Matrix and Output Polarity outlined below. To maximize recovery from programming errors, leave all links of unused gates intact.

SET-UP

Terminate all device outputs with a 10KΩ resistor to +5V.

Output Polarity

PROGRAM ACTIVE HIGH (Fp FUNCTION)

Program output polarity before programming inputs (for convenience). Program one output at a time. (L) links of unused outputs are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Raise V_{CC} (pin 28) from V_{CCV} to V_{CCP}.
B. After t_D delay, force output to be programmed to V_{OPF}.
C. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.
D. After t_D delay, remove V_{OPF} voltage source from output being programmed.
E. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
F. Repeat steps A through E for any other output.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. After t_D delay, set the $\overline{CE}$ input to V_{IL}.
B. Verify output polarity by sensing the logic state of outputs F_0 through F_8. All outputs at a low logic level are programmed active low ($\overline{Fp}$ function), while all outputs at a high logic level are programmed active high (F_p function).

Input Matrix

PROGRAM INPUT VARIABLE

Program one input at a time for one gate at a time. Input variable links of unused gates are not required to be fused. However, unused input variables must be programmed at Don't Care for all used gates.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A-1. If a gate contains nether I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both links by executing both steps A-2 and A-3, before continuing with step C.
A-2. If a gate contains I_0, set to fuse link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step B.
A-3. If a gate contains $\overline{I_0}$, set to fuse link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step B.
B-1. After t_D delay, raise V_{CC} from V_{CCV} to V_{CCP}.
B-2. After t_D delay, force output of gate to be programmed to V_{OPF}.
B-3. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IL} for a period t_p.
B-4. After t_D delay, remove V_{OPF} voltage source from output of gate being programmed.
B-5. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
C. Disable programmed input by returning I_0 to V_{IX}.
D. Repeat steps A through C for all other input variables.
E. Repeat steps A through D for all other gates to be programmed.
F. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

Unambiguous verification of the logic state programmed for the inputs of each gate requires prior knowledge of its programmed output polarity. Therefore, the output polarity verify procedure must precede input variable verify.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Enable all outputs by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Interrogate input variable I_0 as follows: Lower the input voltage to I_0 from V_{IX} to V_{IL}, and sense the logic state of outputs F_{0-8}.

Raise the input voltage to I_0 from V_{IL} to V_{IH} and sense the logic state of outputs F_{0-8}.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

The state of I_O contained in each gate is determined in accordance with the given truth table. Note that 2 tests are required to uniquely determine the state of the input variable contained in each gate.

B. Disable verified input by returning I_O to V_{IX}.

C. Repeat steps A and B for all other input variables.

D. Remove V_{IX} from all input variables.

TRUTH TABLE FOR INPUT VERIFICATION

I_O	F_P	$\overline{F_P}$	INPUT VARIABLE STATE
0	1	0	$\overline{I_O}$
1	0	1	
0	0	1	I_O
1	1	0	
0	1	0	Don't care
1	1	0	
0	0	1	(I_O), ($\overline{I_O}$)
1	0	1	

PROGRAMMING SYSTEMS SPECIFICATIONS[1] $T_A = 25°C$

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	V_{CC} supply					V
V_{CCP}	Program[2]	I_{CCP} = 550mA, min Transient or steady state	8.25	8.5	8.75	
V_{CCV}	Verify		4.75	5.0	5.25	
I_{CCP}	I_{CC} limit (program)	V_{CCP} = +8.5 ± .25V, Transient or steady state	550		1,000	mA
V_{OPF}	Forced output voltage[3] (program)	I_{OP} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Output current (program)	V_{OP} = +17 ± 1V, Transient or steady state	275	300	325	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			10.0	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			10.0	mA
T_R	Output pulse rise time	10% to 90%	10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				100	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

1. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of a gate output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

LOGIC PROGRAMMING

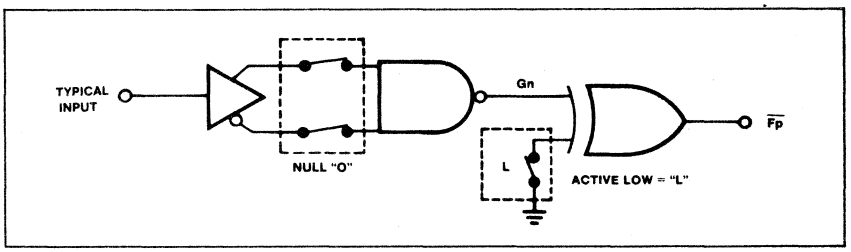
In a virgin device all Ni-Cr links are intact. The initial programmed state of each gate is shown in the Typical Gate illustration.

The FPGA can be programmed by means of Logic programming equipment.

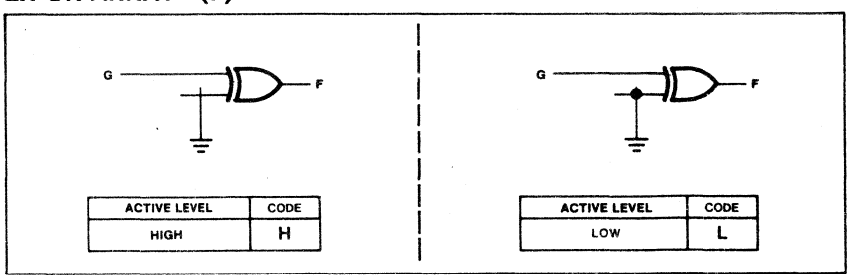
With Logic programming, the AND/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table, the logic state or action of variables I and F associated with each gate G_n is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

TYPICAL GATE



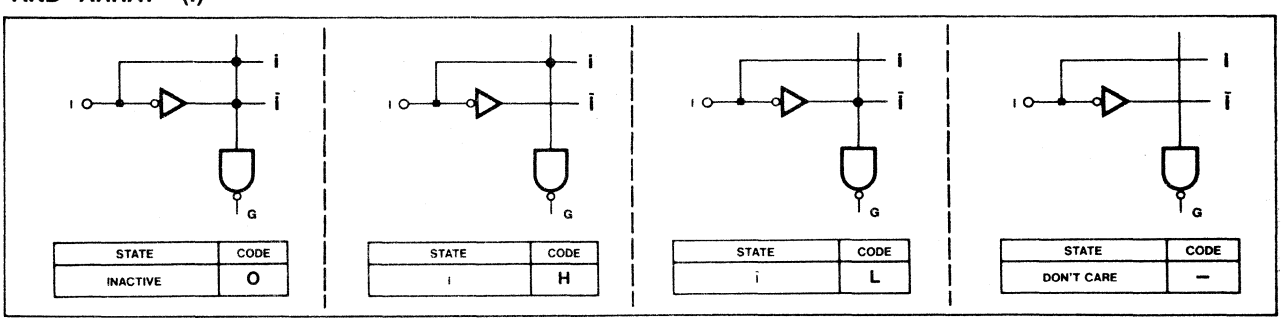
EX-OR ARRAY - (F)



ACTIVE LEVEL	CODE
HIGH	H

ACTIVE LEVEL	CODE
LOW	L

"AND" ARRAY - (I)



STATE	CODE
INACTIVE	O

STATE	CODE
I	H

STATE	CODE
$\bar{I}$	L

STATE	CODE
DON'T CARE	–

NOTES
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates G_n.
2. Any gate G_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

FPGA PROGRAM TABLE (Logic)

CUSTOMER NAME _____	*THIS PORTION TO BE COMPLETED BY SIGNETICS*
PURCHASE ORDER # _____	*CF (XXXX)* _____
SIGNETICS DEVICE # _____	*CUSTOMER SYMBOLIZED PART #* _____
TOTAL NUMBER OF PARTS _____	*DATE RECEIVED* _____
PROGRAM TABLE # _____	*COMMENTS* _____

F_0 = _____

F_1 = _____

F_2 = _____

F_3 = _____

F_4 = _____

F_5 = _____

F_6 = _____

F_7 = _____

F_8 = _____

GATE		INPUT VARIABLE															
ACTIVE LEVEL		I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
F_0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_1	16	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F_2	32	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
F_3	48	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
F_4	64	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
F_5	80	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
F_6	96	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
F_7	112	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
F_8	128	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
Active–High = H Active–Low = L		I_m = H		$\overline{I_m}$ = L		Don't Care = –											

NOTES

1. The number in each cell in the table denotes its address for programmers with a decimal address display.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

FPGA PROGRAM TABLE (Memory)[1,2]

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE ____

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

MEMORY PROGRAMMING

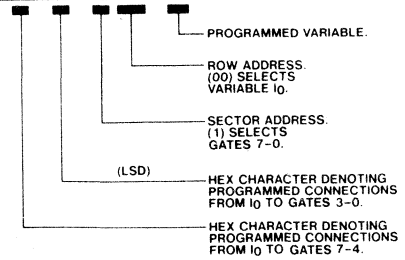
The FPGA can also be programmed with Memory programming equipment, in conunction with the FPGA logic diagram. With Memory programming, all links at the AND and EX-OR array cross-points are treated as memory locations with row-sector addresses. Rows are consecutively scanned while each sector addresses eight gates G_n simultaneously. All necessary gate connections are first translated from logic equations as "dot" connections at appropriate locations on the logic diagram. The "dot" connection pattern is then transferred to the corresponding Variable-Address locations on the Program Table using (0) = "dot", (1) = blank in a HEX format:

PROGRAMMING DEFINITIONS

LINK	STATUS	CODE
⊕ or ✳	CLOSED	0
┼	OPEN	1

TYPICAL TABLE ENTRY

SECTOR DATA	ADDRESS	VAR
5 : A	1 00	I_0



SECTOR DATA	ADDRESS	ACTIVE LEVEL[3]
:	000	F7-F0
0 :	001	F8

SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	VAR[4,5]
0 :	200	:	100	I_0
0 :	201	:	101	
0 :	202	:	102	I_1
0 :	203	:	103	
0 :	204	:	104	I_2
0 :	205	:	105	
0 :	206	:	106	I_3
0 :	207	:	107	
0 :	208	:	108	I_4
0 :	209	:	109	
0 :	20A	:	10A	I_5
0 :	20B	:	10B	
0 :	20C	:	10C	I_6
0 :	20D	:	10D	
0 :	20E	:	10E	I_7
0 :	20F	:	10F	
0 :	210	:	110	I_8
0 :	211	:	111	
0 :	212	:	112	I_9
0 :	213	:	113	
0 :	214	:	114	I_{10}
0 :	215	:	115	
0 :	216	:	116	I_{11}
0 :	217	:	117	
0 :	218	:	118	I_{12}
0 :	219	:	119	
0 :	21A	:	11A	I_{13}
0 :	21B	:	11B	
0 :	21C	:	11C	I_{14}
0 :	21D	:	11D	
0 :	21E	:	11E	I_{15}
0 :	21F	:	11F	

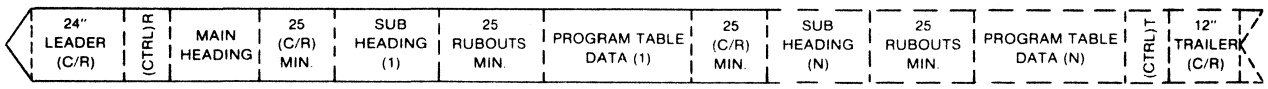
NOTES:

1. All HEX addresses denote programmable links at Row-Sector locations as shown on the FPGA logic diagram. Sector data specifies the programmed state of fusible links coupling the indicated variable to designated sets of gates. These are sectioned from left to right in HIGH and LOW groups of 4, to which HEX data is assigned in accordance with the definitions below. The LOW group corresponds to least significant HEX digit. Since sector 2 contains a single gate, legal data entries are limited to "00" and "01".
2. Since memory programmers display a continuous address field, 3 "empty" address fields exist between program table sectors, such as (002-OFF), (120-1FF), (220-2FF), etc. The only entry allowed in these fields is "00".
3. Active level data for output F8 is assigned at address (001), for which legal data entries are limited to "00" and "01".
4. Even row addresses in the AND array correspond to links i.
5. Odd row addresses in the AND array correspond to links $\bar{i}$.

TWX TAPE CODING

The FPGA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



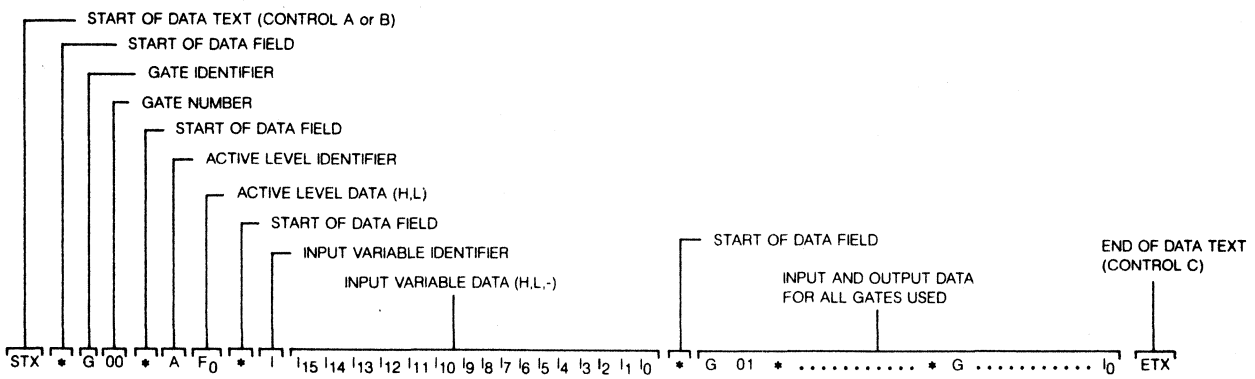
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks in Logic format are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level and AND gates information separated by appropriate identifiers in accordance with the following sequence:



Entries for the 2 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_M	$\overline{I_M}$	Don't care
H	L	— (dash)

NOTE
Enter (—) for unused inputs of used gates.

OUTPUT ACTIVE LEVEL	
Active high	Active low
H	L

NOTES
1. Polarity programmed once only.
2. Enter (L) for all unused outputs.

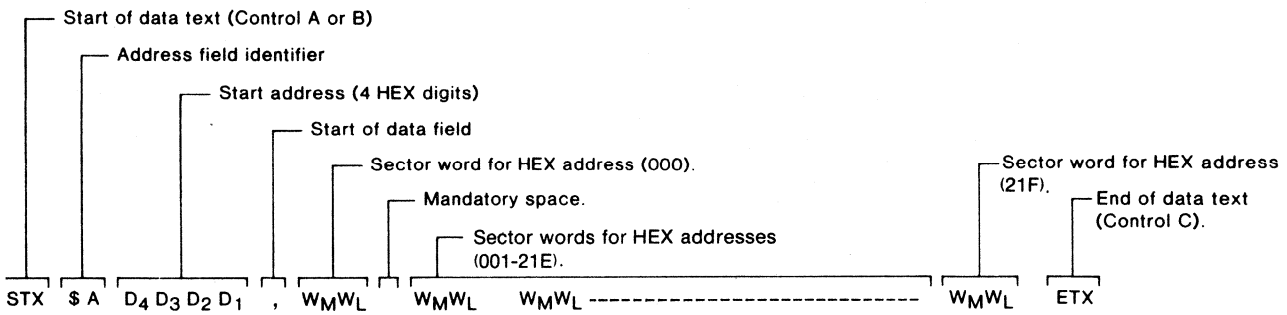
Although AND Gate data are shown entered in sequence, this is not necessary. It is possible to input only one Gate if desired. Unused Gates require no entry. ETX signalling end of Program Table may occur with less than the maximum number of AND Gates entered.

NOTES
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk(*).
4. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

D. Program Table data blocks in MEMORY format are initiated with an STX character, and terminated with an ETX character.

Carriage return and line feed can be interspersed to achieve any preferred teletype printout from tape.

The body of the data consists of address/data information in accordance with the following ASCII-HEX (Space) format. Address field delimiters may be used to skip over "empty" sector areas:



Entries in the data field are made in groups of 8 bits. These are specified with hexadecimal characters W_MW_L followed by a space to separate sequential address entries. In each 8-bit word W_M specifies the most significant 4 bits and W_L designates the least significant 4 bits.

Other ASCII-HEX formats (Percent, Apostrophe, Comma, etc.) are also acceptable. To insure compatibility with other formats consult Signetics or your programmer manual.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S104 (open collector outputs) and the 82S105 (tri-state outputs) are bipolar, programmable state machines of the Mealy type. They contain logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output registers. These consist respectively of 6 Q_P, and 8 Q_F edge triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_{0\text{-}15}$ with 6 internal inputs $P_{0\text{-}5}$ fed back from the State register to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement array. Also, if desired, the Preset input can be converted to $\overline{\text{Output-Enable}}$ function, as an additional user programmable option.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S104/105, F or N, and for the military temperature range (−55°C to +125°C) specify S82S104/105, F, I, G or R.

FEATURES

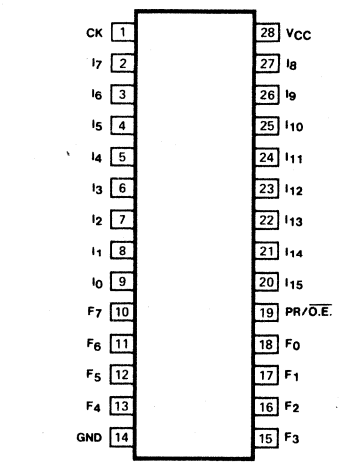
- Field programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-BIT state register
- 8-BIT output register
- Transition complement array
- Positive edge trigger clock
- Programmable asynchronous preset or output enable
- Power-on preset to all "1" of internal registers
- 90ns maximum I/O delay
- 650mW power dissipation (typical)
- TTL compatible
- Single +5V supply

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems

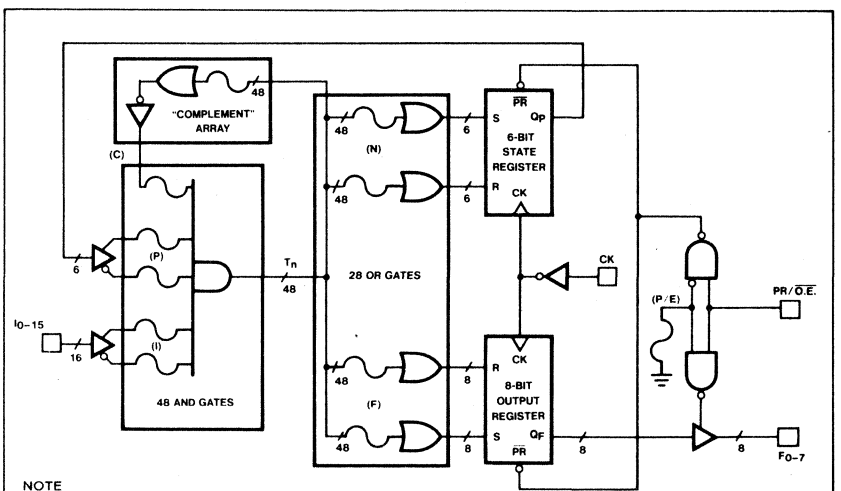
PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip I = Ceramic R = Flat Pack
N = Plastic G = Leadless

BLOCK DIAGRAM



NOTE
I, P, C, N, F and P/E are user programmable connections.

TRUTH TABLE (Output Control)

I_0	INPUT OPTION		F_N
	PR	$\overline{\text{O.E.}}$	
*	H		H
+10V	L		Q_P
X	L		Q_F
*		H	H/Hi-Z
+10V		L	Q_P
X		L	Q_F

NOTES
1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C\ (I_0\ I_1\ I_2 \ldots)\ (P_0\ P_1 \ldots P_5)$
2. Either Preset (active-High) or $\overline{\text{Output Enable}}$ (active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V
6. X = Don't Care (≤5.5V)

TRUTH TABLE (All flip-flops)

V_{CC}	INPUT OPTION		CK	S	R	STATE REGISTER	OUTPUT REGISTER
	PR	$\overline{\text{O.E.}}$				Q_P	Q_F
+5V	H		X	X	X	H	H
	L	X	↑	L	L	Q_P	Q_F
	L	X	↑	L	H	L	L
	L	X	↑	H	L	H	H
	L	X	↑	H	H	INDET.	INDET.
↑	X	X	X	X	X	H	H

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

PIN DESIGNATION

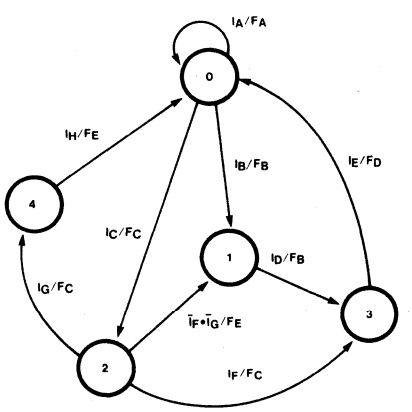
PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**CLOCK** The clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
[2-8 20-27]	I_{1-15}	**LOGIC INPUTS** The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High
9	I_0	**LOGIC/DIAGNOSTIC INPUT** A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-5} reflect the contents of State Register bits P_{0-5}. The contents of the Output Register remain unaltered.	Active-High
[10-13 15-18]	F_{0-7}	**LOGIC/DIAGNOSTIC OUTPUTS** Eight device outputs which normally reflect the contents of Output Register bits Q_{0-5}, when enabled. When I_0 is held at +10V, $F_{0-5} = (P_{0-5})$, and $F_{6,7}$ = Logic "1".	Active-High/Low (user defined)
19	PR/$\overline{O.E.}$	**PRESET OR $\overline{\text{OUTPUT ENABLE}}$ INPUT** A user programmable function: • **PRESET** Provides an asynchronous preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F_{0-7} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low. • **$\overline{\text{OUTPUT ENABLE}}$** Provides an output enable function to buffers F_{0-7} from the Output Register.	Active-High Active-Low

PROGRAMMABLE VARIABLES

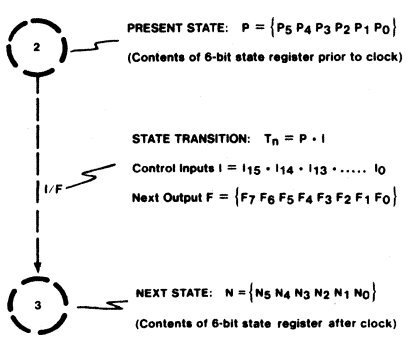
The FPLS can be programmed with any clocked sequence expressed in terms of "control" variables, which are coupled to on-chip gates and flip-flops by means of programmable connections through Ni-Cr fusible links:

(I) - External control inputs for state jump conditions.
(P) - Present state, prior to clock.
(C) - Complement variable for activating and generating the complement of programmed jump conditions.
(T_n) - Transition "AND" terms including I, P.
(N) - Next state, following clock.
(F) - Next logic output, following clock.
(P/E) - Asynchronous preset, or output enable function.

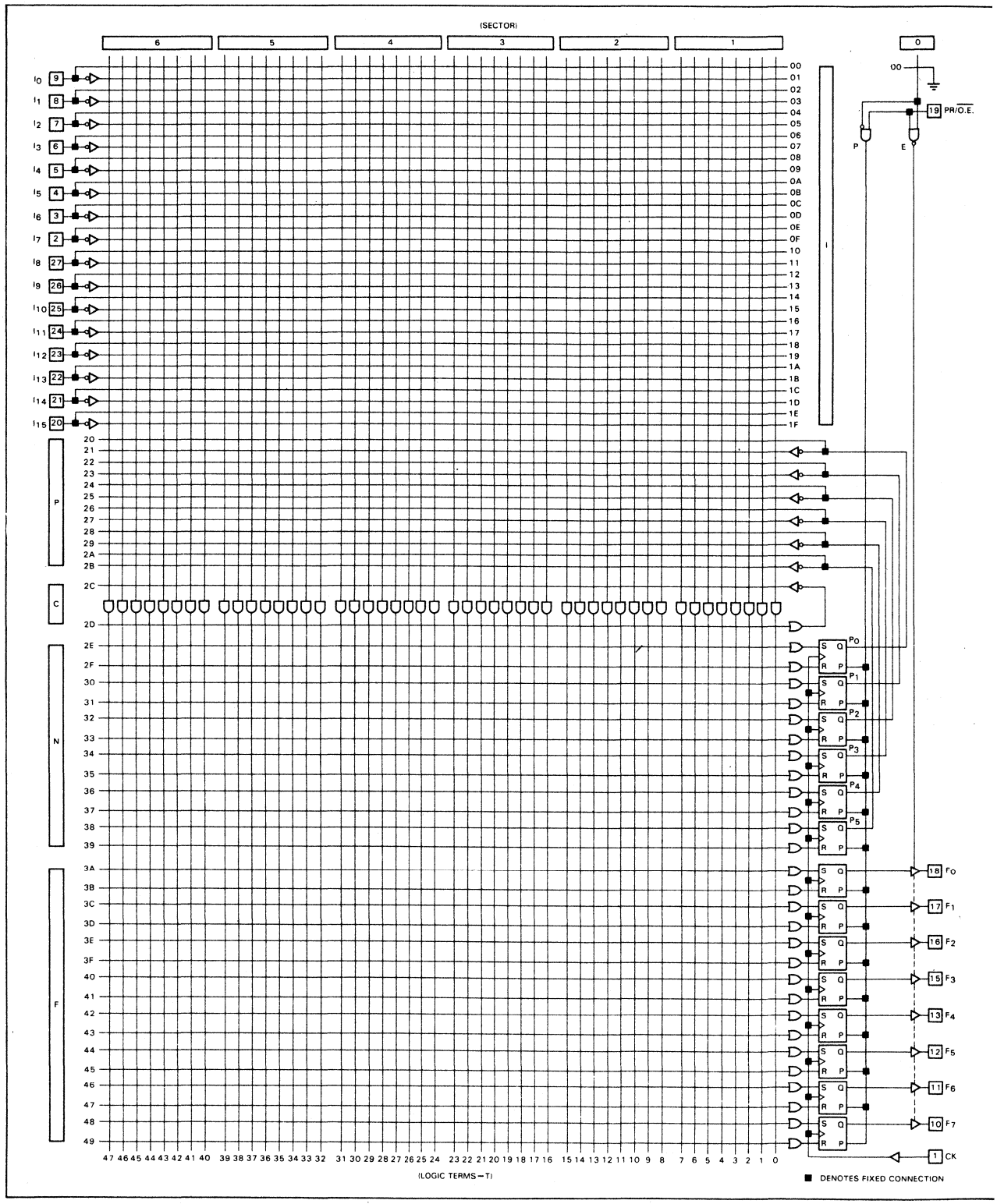
TYPICAL STATE DIAGRAM



TYPICAL STATE TRANSITION



FPLS LOGIC DIAGRAM



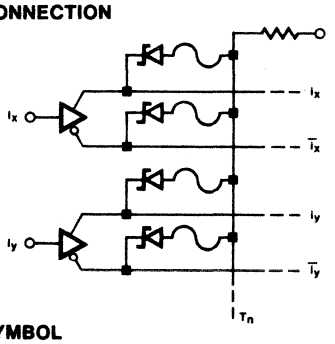
OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

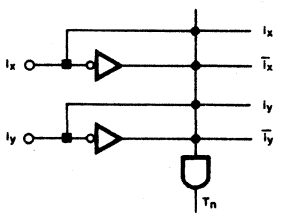
PROGRAMMABLE CONNECTIONS (■ Denotes fixed connection)

"AND" ARRAY (TYPICAL)

CONNECTION

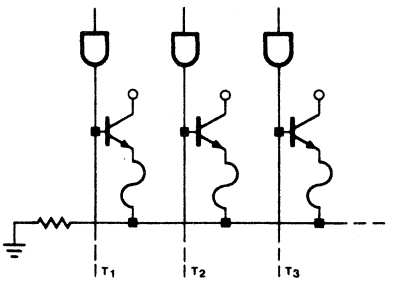


SYMBOL

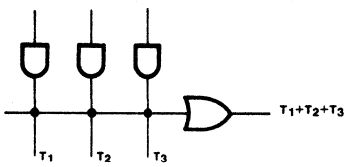


"OR" ARRAY (TYPICAL)

CONNECTION

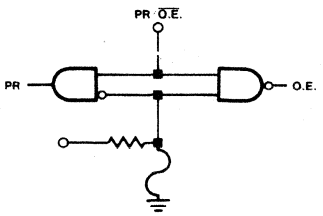


SYMBOL

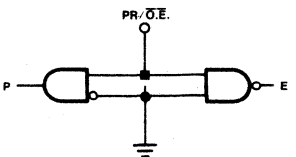


PR/$\overline{O.E.}$ OPTION

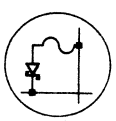
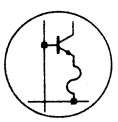
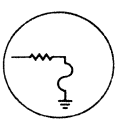
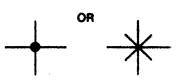
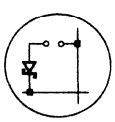
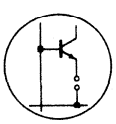
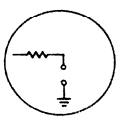
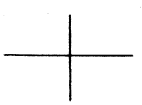
CONNECTION



SYMBOL



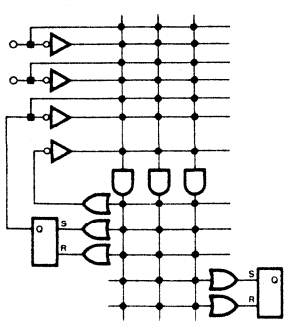
PROGRAMMING LEGEND

AND	OR	PR/$\overline{O.E.}$	LINK	SYMBOL
			CLOSED	
			OPEN	

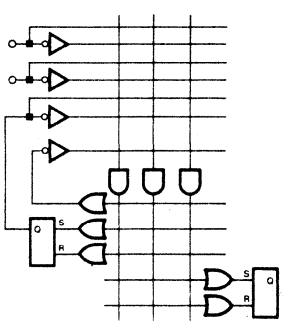
VIRGIN DEVICE

The FPLS is shipped with all internal links intact, so that a "dot" connection exists at all cross points in all arrays. For clarity, unprogrammed arrays are initially shown blank. The desired functional logic diagram is obtained by placing "dot" connections in used device areas where links remain intact. (Since both True and Complement input links of all AND gates are initially closed, all gates are disabled, preventing clocking. For testing purposes, clocking can occur via a factory programmed Test Array.

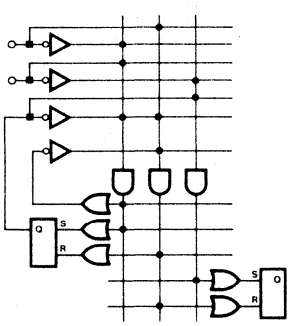
VIRGIN (PARTIAL)



SYMBOL



PROGRAMMED (TYPICAL)



FPLS ARCHITECTURE

The 82S104/105 Logic Sequencer is a programmable state machine of the Mealy type, in which the output is a function of the present state and the present input.

With the FPLS a user can program any logic sequence expressed as a series of jumps between stable states, triggered by a valid input condition (I) at clock time (t). All stable states are arbitrarily assigned and stored in the State Register. The logic output of the machine is also programmable, and is stored in the Output Register.

CLOCKED SEQUENCE

A synchronous logic sequence can be represented as a group of circles interconnected with arrows. The circles represent stable states, labeled with an arbitrary numerical code (binary, hex, etc.) corresponding to discrete states of a suitable register. The arrows represent state transitions, labeled with symbols denoting the jump condition and the required *change* in output. The number of states in the sequence depends on the length and complexity of the desired algorithm.

STATE JUMPS

The state from which a jump originates is referred as the present state (P), and the state to which a jump terminates is defined as the next state (N). A state jump always causes a change in state, but may or may not cause a change in machine output (F).

State jumps can occur only via "transition terms" T_n. These are logical AND functions of the clock (t), the present state (P), and a valid input (I). Since the clock is actually applied to the State Register, $T_n = I \bullet P$. When T_n is "true", a control signal is generated and used at clock time (t) to force the contents of the State Register from (P) to (N), and to change the contents of the Output Register (if necessary). The simple state jump below, involving 2 inputs, 1 state bit, and 1 output bit, illustrates the equivalence of discrete and programmable logic implementations.

FPLS LOGIC STRUCTURE

The FPLS consists of programmable AND and OR gate arrays which control the Set and Reset inputs of a State Register, as well as monitor its output via an internal feedback path. The arrays also control an independent Output Register, added to store output commands generated during state transitions, and to hold the output constant during state sequences involving no output changes. If desired, any number of bits of the Output Register can be used to extend the width of the State Register, via external feedback.

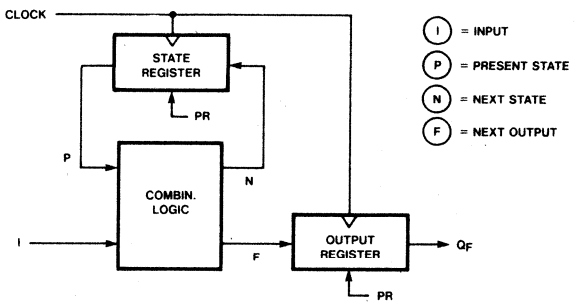


Figure 1: Basic architecture of 82S104/105 FPLS. I, P, N, and F are multi-line paths denoting groups of binary variables programmed by the user.

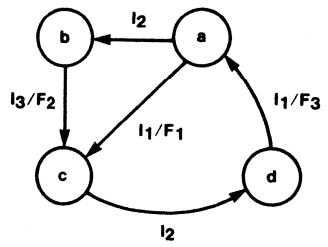


Figure 2: Typical state diagram. I_{1-3} are jump conditions which must be satisfied before any transitions take place. F_f are changes in output triggered by I_m, and stored in the Output Register. State transitions a→b and c→d involve no output change.

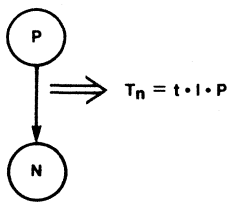


Figure 3: Typical state transition between any two states of Figure 2. The arrow connecting the two states gives rise to a transition term T_n. I is the jump condition.

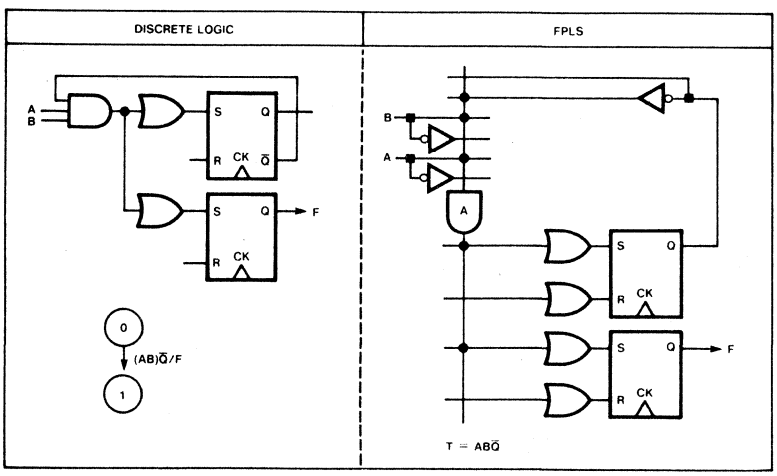


Figure 4: Typical state jump from state (0) to state (1), if inputs A="1". The jump also forces F="1", as required.

SIMPLIFIED LOGIC DIAGRAM OF
82S104/105 FPLS.

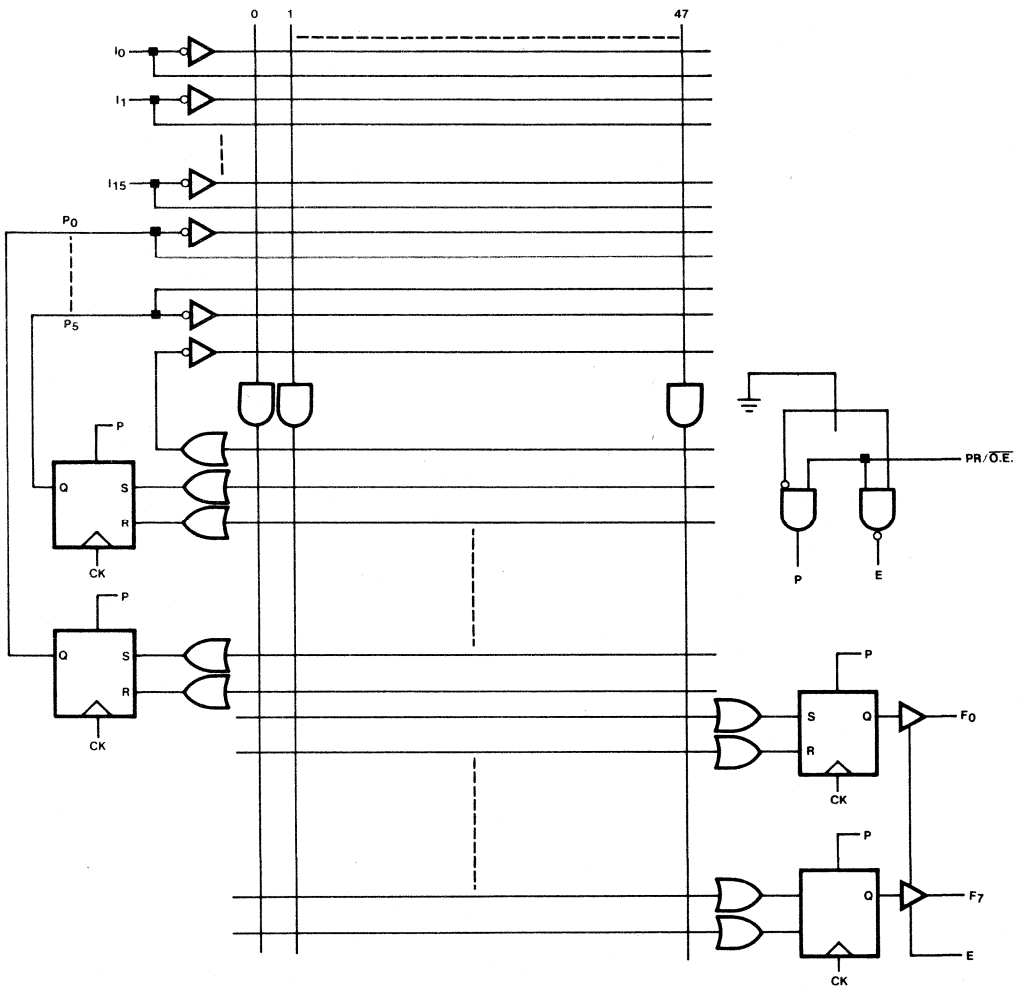


Figure 5

NPUT BUFFERS

16 external inputs (I_m) and 6 internal inputs (P_s), fed back from the state register, are combined in the AND array through two sets of True/Complement (T/C) buffers. There are a total of 22 T/C buffers, all connected to multi-input AND gates via fusible links which are initially intact.

Selective fusing of these links allows coupling either True, Complement, or Don't Care values of (I_m) and (P_s).

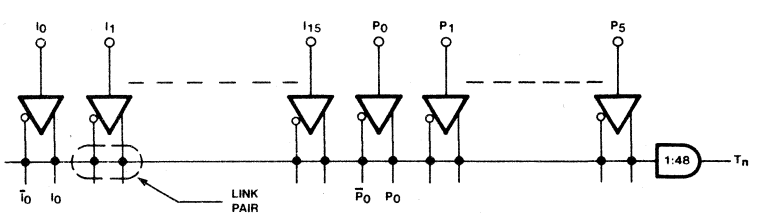


Figure 6: Typical AND gate coupled to (I) and (P) inputs. If at least one link *pair* remains intact, T_n is unconditionally forced Low.

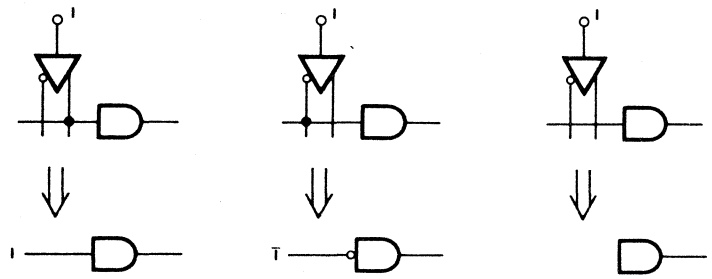


Figure 7: Choice of input polarity coupling to a typical AND gate. With both links open, (I) is logically Don't Care.

"AND" ARRAY

State jumps and output changes are triggered at clock time by valid transition terms T_n. These are logical AND functions of the present state (P) and the present input (I).

The FPLS AND array contains a total of 48 AND gates. Each gate has 45 inputs—44 connected to 22 T/C input buffers, and 1 dedicated to the Complement Array. The outputs of all AND gates are propagated through the OR array, and used at clock time (t) to force the contents of the State Register from (P) to (N). They are also used to control the Output Register, so that the FPLS 8-bit output F_f is a function of the inputs and present state.

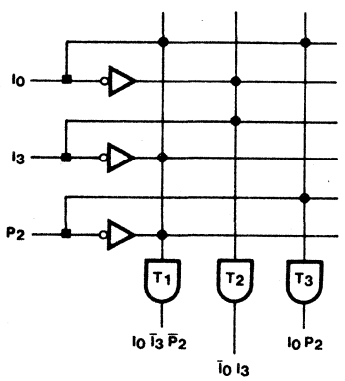


Figure 8: Typical transition terms involving arbitrary inputs and state variables. All remaining gate inputs are programmed Don't Care. Note that T_2 output is state independent.

"OR" ARRAY

In general, a clocked sequence will consist of several stable states and transitions, as determined by the complexity of the desired algorithm. All state and output changes in the state diagram imply changes in the contents of state and output registers.

Thus, each flip-flop in both registers may need to be conditionally set or reset several times with T_n commands. This is accomplished by selectively ORing through programmable OR array all AND gate outputs T_n necessary to activate the proper flip-flop control inputs.

The FPLS OR array consists of 14 pairs of OR gates, controlling the S/R inputs of 14 state and output register stages, and a single OR gate for the Complement Array. All gates have 48 inputs for connecting to all 48 AND gates.

COMPLEMENT ARRAY

The COMPLEMENT array provides an asynchronous feed back path from the OR array back to the AND array.

This structure enables the FPLS to perform both direct and complement sequential state jumps with a minimum of transition (AND) terms.

Typically direct jumps, such as T_1 and T_2 in Figure 11 require only a single AND gate each.

But a complement jump such as T_3 generally requires many AND gates if implemented as a direct jump. However, by using the complement array, the logic requirements for this type of jump can be handled with just one more gate from the AND array.

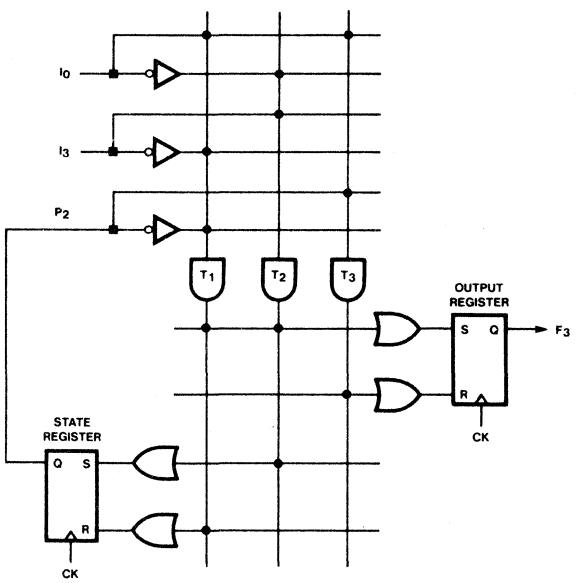


Figure 9: Typical OR array gating of transition terms $T_{1,2,3}$ controlling arbitrary state and output register stages.

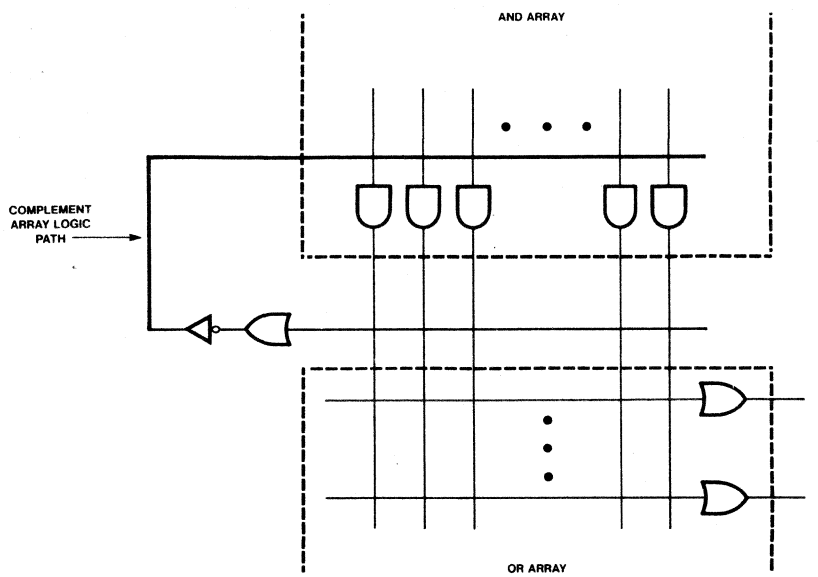
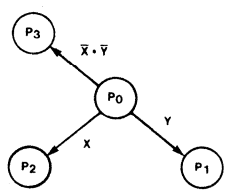


Figure 10: The COMPLEMENT array is logically constructed from a 48-input programmable OR gate followed by an inverter. All AND terms coupled to the OR gate are complemented at the inverter output, and can be fed back as inputs to the AND array.

As indicated in Figure 12, the single complement array gate may be used for many states of the state diagram. This happens because all transition terms linked to the OR gate include the present state as a part of their conditional logic. In any particular state only those transition terms which are a function of that state are enabled; all other terms coupled to different states are disabled and do not influence the output of the complement array. As a general rule of thumb, the complement array can be used as many times as there are states.

(A) TYPICAL STATE SEQUENCE



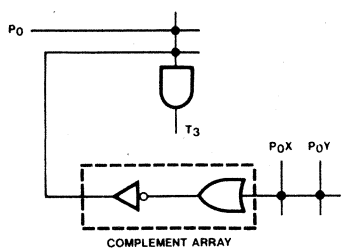
TRANSITION TERMS

DIRECT

$T_1 = P_0X$

$T_2 = P_0Y$

(B) COMPLEMENT JUMP



$T_3 = P_0(\overline{P_0X + P_0\overline{Y}})$

$T_3 = P_0[\overline{P_0(\overline{X} + Y)}]$

$T_3 = P_0[\overline{P}_0 + \overline{(\overline{X} + Y)}]$

$T_3 = 0 + P_0\overline{(\overline{X} + Y)}$

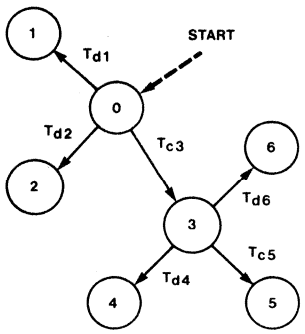
$T_3 = P_0(\overline{X} \cdot \overline{Y})$

COMPLEMENT

$T_3 = P_0(\overline{X} \cdot \overline{Y}) = P_0(\overline{T_1 + T_2})$

Figure 11: (A) X and Y specify the conditional logic for direct jump transition terms T_1 and T_2. The complement jump term T_3 is true only when both T_1 and T_2 are false. (B) Note that the complementary logic expression for T_3, $\overline{T_1 + T_2}$, corresponds exactly to the logic structure of the complement array.

(A) STATE DIAGRAM



(B) LOGIC DEFINITION

$T_{d1} = I_0\bar{I}_1P_0$

$T_{d2} = I_2P_0$

$T_{c3} = \overline{(\bar{T}_{d1} + T_{d2})}P_0 = \overline{(I_0\bar{I}_1 + I_2)}P_0$

$T_{d4} = \bar{I}_2P_3$

$T_{d6} = I_0I_1P_3$

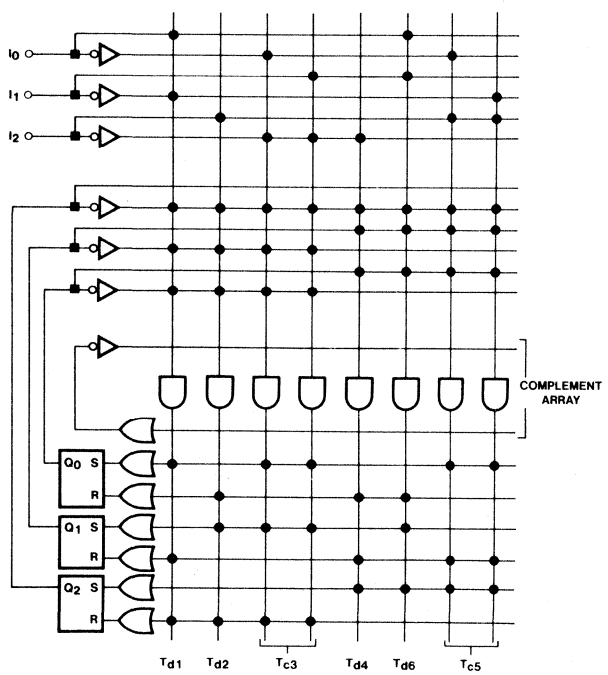
$T_{c5} = \overline{(T_{d4} + T_{d6})}P_3 = \overline{(I_0I_1 + \bar{I}_2)}P_3$

T_{cn} = COMPLEMENT STATE TRANSITION TERM

T_{dn} = DIRECT STATE TRANSITION TERM

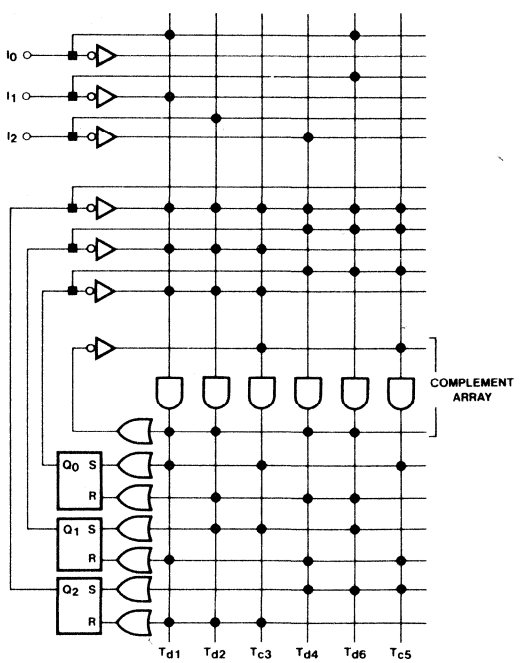
P_s = PRESENT STATE

(C) STATE LOGIC WITHOUT USING THE COMPLEMENT ARRAY



8 TRANSITION TERMS USED

(D) STATE LOGIC USING THE COMPLEMENT ARRAY



6 TRANSITION TERMS USED

Figure 12: Logic reduction with the complement array. The logic state diagram in (a) includes complement jumps T_{C3} and T_{C5} defined in (b). When using the complement array a savings of 2 transition terms results, as shown in (c) and (d).

BJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

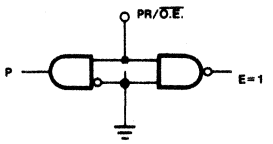
OGIC PROGRAMMING

ıe FPLS can be programmed by means of ɔgic programming equipment.

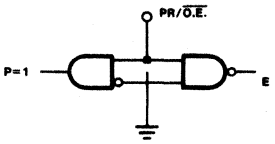
'ith Logic programming, the AND/OR gate put connections necessary to implement ıe desired logic function are coded directly om the State Diagram using the Program ıble on the following page.

this Table, the logic state or action of ɔntrol variables C, I, P, N, and F, associat-d with each Transition Term T_n, is assigned symbol which results in the proper fusing ıttern of corresponding link pairs, defined s follows:

PRESET/$\overline{O.E.}$ OPTION - (P/E)

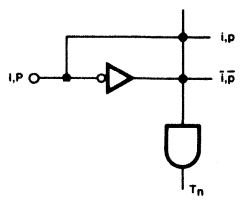


OPTION	CODE
PRESET	H

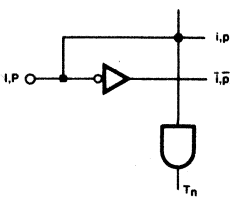


OPTION	CODE
$\overline{O.E.}$	L

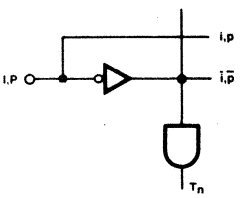
AND" ARRAY - (I), (P)



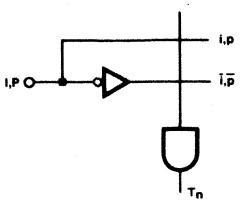
STATE	CODE
INACTIVE 1,2	O



STATE	CODE
I,P	H

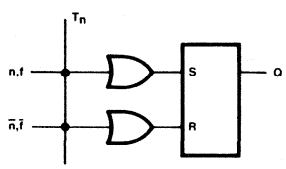


STATE	CODE
$\bar{i},\bar{p}$	L

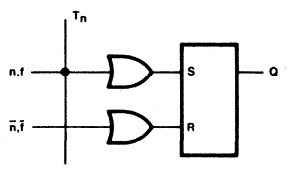


STATE	CODE
DON'T CARE	—

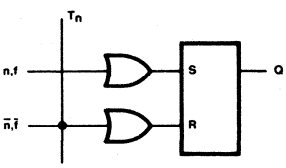
OR" ARRAY - (N), (F)



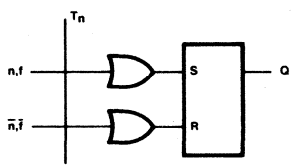
ACTION	CODE
INACTIVE 1,3	O



ACTION	CODE
SET	H

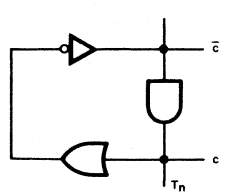


ACTION	CODE
RESET	L

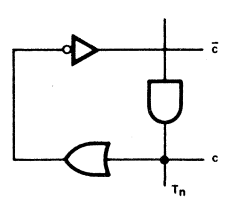


ACTION	CODE
NO CHANGE	—

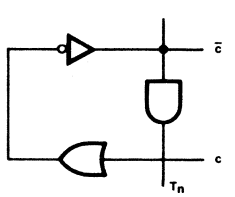
'COMPLEMENT ARRAY" - (C)



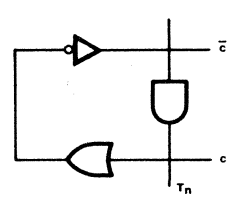
ACTION	CODE
INACTIVE 1,4	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	—

IOTES

. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.

. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.

3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGI(
SERIES 28

FPLS PROGRAM TABLE (Logic)

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV _____ DATE _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

PROGRAM TABLE ENTRIES:

Cn		Im, Ps		Ns, Fr		P/E	
GENERATE	A	I, P	H	SET	H	PRESET	H
PROPAGATE	•	$\bar{I}$, $\bar{P}$	L	RESET	L	$\overline{O.E.}$	L
TRANSPARENT	—	DON'T CARE	—	NO CHANGE	—		

NOTES

1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead f clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (—).
3. Unused transition and output Terms can be left blank.
4. Letters in variable fields are used as identifiers by logic type programmers.

	TRANSITION TERM																	OPTION (P/E)						
	INPUT VARIABLE (Im)																PRESENT STATE (Ps)	OUTPUT TERM						
																		NEXT STATE (Ns)					OUTPUT FUNCTION (Fr)							
NO.	C_n	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
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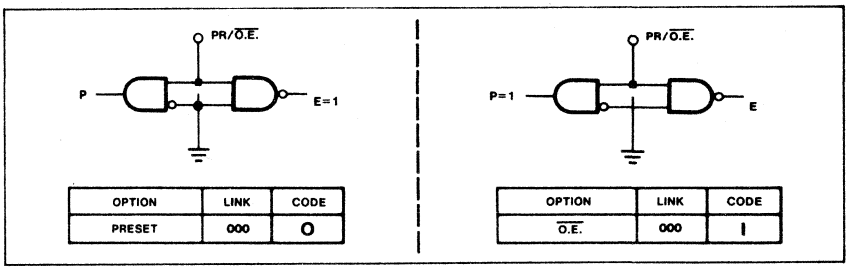
OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

MEMORY PROGRAMMING

The FPLS can also be programmed with Memory programming equipment, using the device logic diagram in conjunction with the Memory Program Table on the following page. With Memory programming, all links at the AND and OR array cross-points are treated as memory locations with row-sector addresses. Rows are consecutively scanned while each sector addresses eight Transition Terms T_n simultaneously. All necessary gate connections are first translated from the State Diagram as "dot" connections at appropriate locations on the logic diagram. The "dot" connection pattern is then transferred to the corresponding Variable-Term locations on the Program Table using (0) = "dot", (1) = blank:

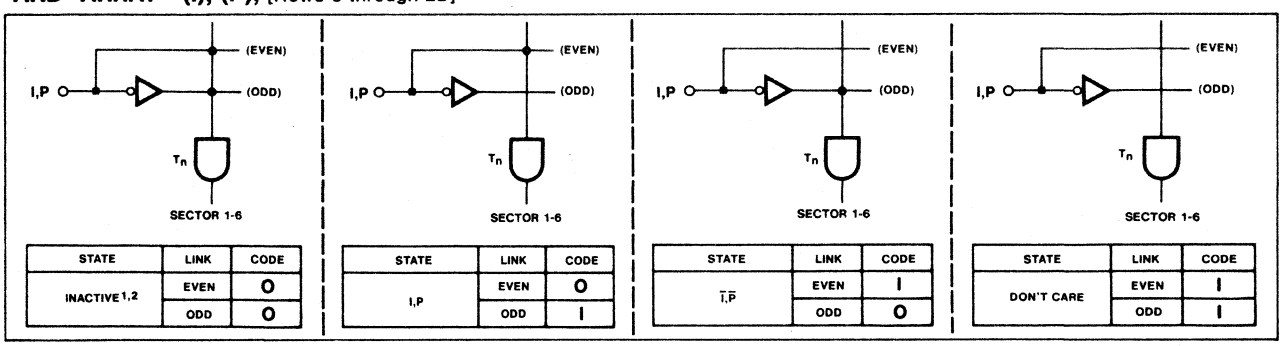
PRESET/$\overline{O.E.}$ OPTION - (P/E)



OPTION	LINK	CODE
PRESET	000	0

OPTION	LINK	CODE
$\overline{O.E.}$	000	1

"AND" ARRAY - (I), (P), [Rows 0 through 2B]



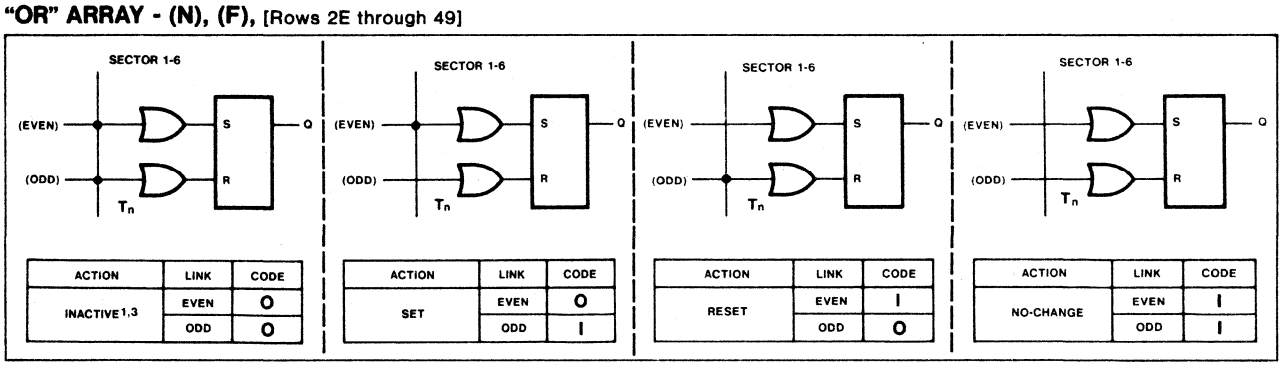
STATE	LINK	CODE
INACTIVE[1,2]	EVEN	0
	ODD	0

STATE	LINK	CODE
I,P	EVEN	0
	ODD	1

STATE	LINK	CODE
$\overline{I,P}$	EVEN	1
	ODD	0

STATE	LINK	CODE
DON'T CARE	EVEN	1
	ODD	1

"OR" ARRAY - (N), (F), [Rows 2E through 49]



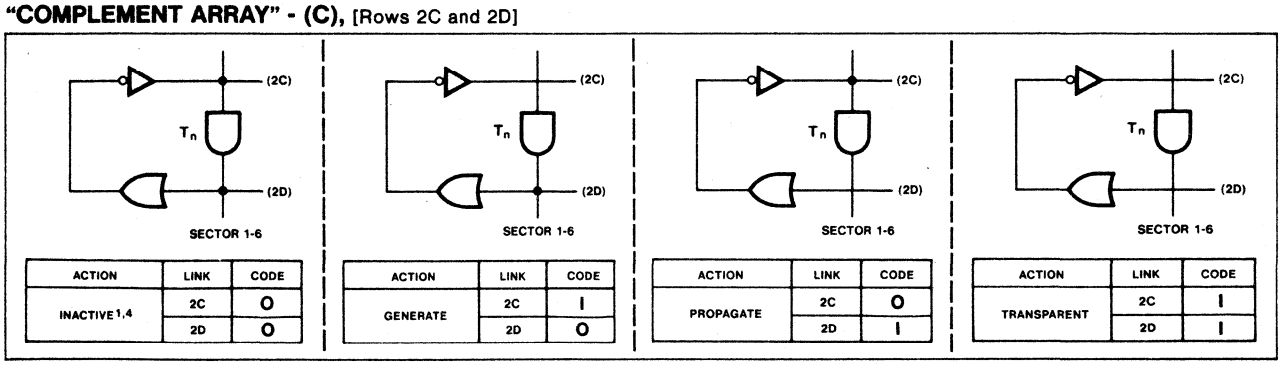
ACTION	LINK	CODE
INACTIVE[1,3]	EVEN	0
	ODD	0

ACTION	LINK	CODE
SET	EVEN	0
	ODD	1

ACTION	LINK	CODE
RESET	EVEN	1
	ODD	0

ACTION	LINK	CODE
NO-CHANGE	EVEN	1
	ODD	1

"COMPLEMENT ARRAY" - (C), [Rows 2C and 2D]



ACTION	LINK	CODE
INACTIVE[1,4]	2C	0
	2D	0

ACTION	LINK	CODE
GENERATE	2C	1
	2D	0

ACTION	LINK	CODE
PROPAGATE	2C	0
	2D	1

ACTION	LINK	CODE
TRANSPARENT	2C	1
	2D	1

NOTES

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
2. Any gate T_n will be unconditionally inhibited if both even and odd links of I or P pairs are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

FPLS PROGRAM TABLE (Memory)[1,2]

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV _____ DATE _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

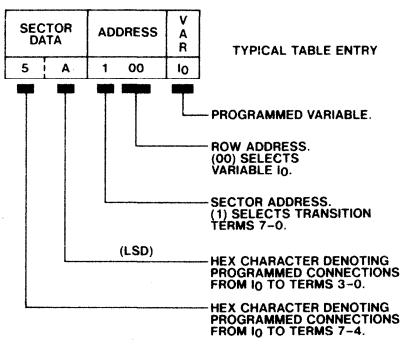
COMMENTS _____

SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	VAR[4,5]
:	600	:	500	:	400	:	300	:	200	:	100	I_0
:	601	:	501	:	401	:	301	:	201	:	101	
:	602	:	502	:	402	:	302	:	202	:	102	I_1
:	603	:	503	:	403	:	303	:	203	:	103	
:	604	:	504	:	404	:	304	:	204	:	104	I_2
:	605	:	505	:	405	:	305	:	205	:	105	
:	606	:	506	:	406	:	306	:	206	:	106	I_3
:	607	:	507	:	407	:	307	:	207	:	107	
:	608	:	508	:	408	:	308	:	208	:	108	I_4
:	609	:	509	:	409	:	309	:	209	:	109	
:	60A	:	50A	:	40A	:	30A	:	20A	:	10A	I_5
:	60B	:	50B	:	40B	:	30B	:	20B	:	10B	
:	60C	:	50C	:	40C	:	30C	:	20C	:	10C	I_6
:	60D	:	50D	:	40D	:	30D	:	20D	:	10D	
:	60E	:	50E	:	40E	:	30E	:	20E	:	10E	I_7
:	60F	:	50F	:	40F	:	30F	:	20F	:	10F	
:	610	:	510	:	410	:	310	:	210	:	110	I_8
:	611	:	511	:	411	:	311	:	211	:	111	
:	612	:	512	:	412	:	312	:	212	:	112	I_9
:	613	:	513	:	413	:	313	:	213	:	113	
:	614	:	514	:	414	:	314	:	214	:	114	I_{10}
:	615	:	515	:	415	:	315	:	215	:	115	
:	616	:	516	:	416	:	316	:	216	:	116	I_{11}
:	617	:	517	:	417	:	317	:	217	:	117	
:	618	:	518	:	418	:	318	:	218	:	118	I_{12}
:	619	:	519	:	419	:	319	:	219	:	119	
:	61A	:	51A	:	41A	:	31A	:	21A	:	11A	I_{13}
:	61B	:	51B	:	41B	:	31B	:	21B	:	11B	
:	61C	:	51C	:	41C	:	31C	:	21C	:	11C	I_{14}
:	61D	:	51D	:	41D	:	31D	:	21D	:	11D	
:	61E	:	51E	:	41E	:	31E	:	21E	:	11E	I_{15}
:	61F	:	51F	:	41F	:	31F	:	21F	:	11F	
:	620	:	520	:	420	:	320	:	220	:	120	P_0
:	621	:	521	:	421	:	321	:	221	:	121	
:	622	:	522	:	422	:	322	:	222	:	122	P_1
:	623	:	523	:	423	:	323	:	223	:	123	
:	624	:	524	:	424	:	324	:	224	:	124	P_2
:	625	:	525	:	425	:	325	:	225	:	125	
:	626	:	526	:	426	:	326	:	226	:	126	P_3
:	627	:	527	:	427	:	327	:	227	:	127	
:	628	:	528	:	428	:	328	:	228	:	128	P_4
:	629	:	529	:	429	:	329	:	229	:	129	
:	62A	:	52A	:	42A	:	32A	:	22A	:	12A	P_5
:	62B	:	52B	:	42B	:	32B	:	22B	:	12B	
:	62C	:	52C	:	42C	:	32C	:	22C	:	12C	C^6
:	62D	:	52D	:	42D	:	32D	:	22D	:	12D	
:	62E	:	52E	:	42E	:	32E	:	22E	:	12E	N_0
:	62F	:	52F	:	42F	:	32F	:	22F	:	12F	
:	630	:	530	:	430	:	330	:	230	:	130	N_1
:	631	:	531	:	431	:	331	:	231	:	131	
:	632	:	532	:	432	:	332	:	232	:	132	N_2
:	633	:	533	:	433	:	333	:	233	:	133	
:	634	:	534	:	434	:	334	:	234	:	134	N_3
:	635	:	535	:	435	:	335	:	235	:	135	
:	636	:	536	:	436	:	336	:	236	:	136	N_4
:	637	:	537	:	437	:	337	:	237	:	137	
:	638	:	538	:	438	:	338	:	238	:	138	N_5
:	639	:	539	:	439	:	339	:	239	:	139	
:	63A	:	53A	:	43A	:	33A	:	23A	:	13A	F_0
:	63B	:	53B	:	43B	:	33B	:	23B	:	13B	
:	63C	:	53C	:	43C	:	33C	:	23C	:	13C	F_1
:	63D	:	53D	:	43D	:	33D	:	23D	:	13D	
:	63E	:	53E	:	43E	:	33E	:	23E	:	13E	F_2
:	63F	:	53F	:	43F	:	33F	:	23F	:	13F	
:	640	:	540	:	440	:	340	:	240	:	140	F_3
:	641	:	541	:	441	:	341	:	241	:	141	
:	642	:	542	:	442	:	342	:	242	:	142	F_4
:	643	:	543	:	443	:	343	:	243	:	143	
:	644	:	544	:	444	:	344	:	244	:	144	F_5
:	645	:	545	:	445	:	345	:	245	:	145	
:	646	:	546	:	446	:	346	:	246	:	146	F_6
:	647	:	547	:	447	:	347	:	247	:	147	
:	648	:	548	:	448	:	348	:	248	:	148	F_7
:	649	:	549	:	449	:	349	:	249	:	149	

SECTOR DATA	ADDRESS	ACTIVE LEVEL[3]
0 :	000	PR/$\overline{OE}$

NOTES:

1. All HEX addresses denote programmable links at Row-Sector locations as shown on the FPLS' logic diagram. Sector data specifies the programmed state of fusible links coupling the indicated variable to designated sets of terms. These are sectioned from left to right in HIGH and LOW groups of 4, to which HEX data is assigned in accordance with the definitions on page 12. The LOW group corresponds to least significant HEX digit.

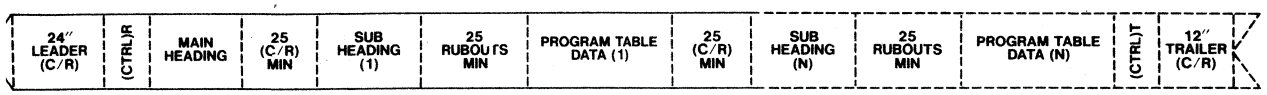


2. Since memory programmers display a continuous address field, 7 "empty" address fields exist between program table sectors, such as (001-OFF), (14A-1FF), (24A-2FF), etc. The only entry allowed in these fields is "00".
3. Active level data for input PR/$\overline{OE}$ is assigned at address (000). Two data entries are allowed: (00) specified the "Preset" option, and "01" specifies the "Output Enable" option.
4. Even row addresses in the AND and OR arrays correspond to links i, p, n, f.
5. Odd row addresses in the AND and OR arrays correspond to links $\bar{i}$, $\bar{p}$, $\bar{n}$, $\bar{f}$.
6. Rows X2C and X2D correspond respectively to links $\bar{c}$ and c of the COMPLEMENT ARRAY.

WX TAPE CODING (LOGIC ORMAT)

e FPLS Program Table can be sent to gnetics in ASCII code format via airmail ing any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however,limit tape length to a roll of 1.75 inch inside diameter and 4.25 inch outside diameter.



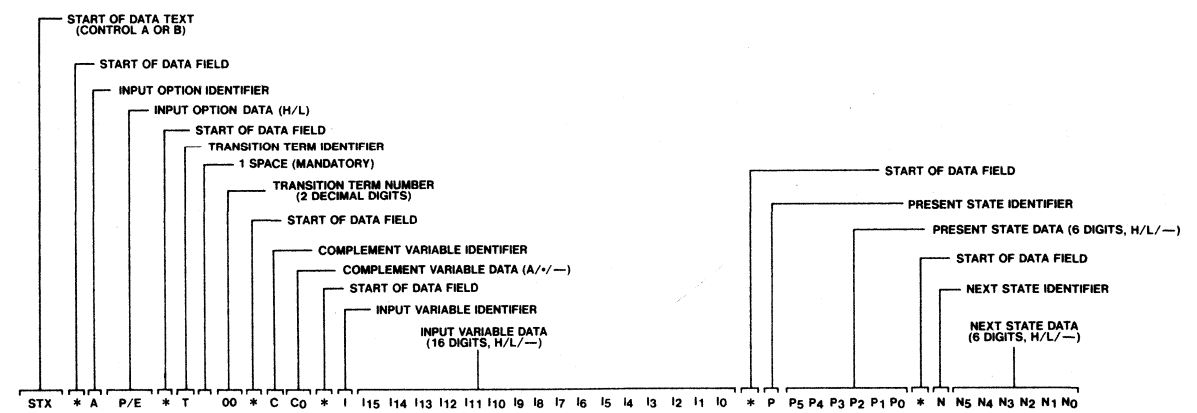
The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

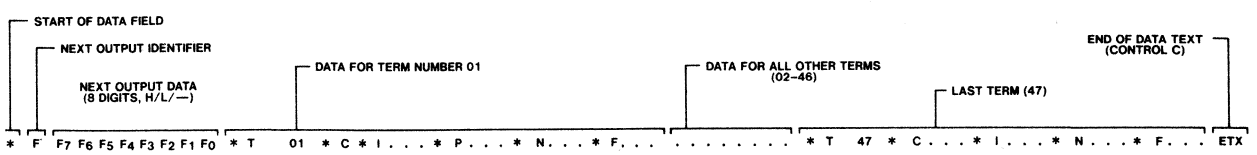
1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of preset/output enable option, transition term, and output term information separated by appropriate identifiers in accordance with the following format:





Entries for the Data Fields are determined in accordance with the following Table:

COMPLEMENT VARIABLE (C)			PRESENT STATE (P_S)/INPUT (I_m)			NEXT STATE (N_S)/OUTPUT (F_n)			OPTION (P/E)	
GENERATE	PROPA-GATE	TRANS-PARENT	I_m, P_S	$\overline{I_m}$, $\overline{P_S}$	DON'T CARE	N_S, F_n	$\overline{N_S}$, $\overline{F_n}$	NO CHANGE	PRESET	OUTPUT ENABLE
A	•	—	H	L	—	H	L	—	H	L

Although the Transition Term data are shown entered in sequence, this is not necessary. It is possible to input only one Transition Term desired. Unused Transition Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number Transition Terms entered.

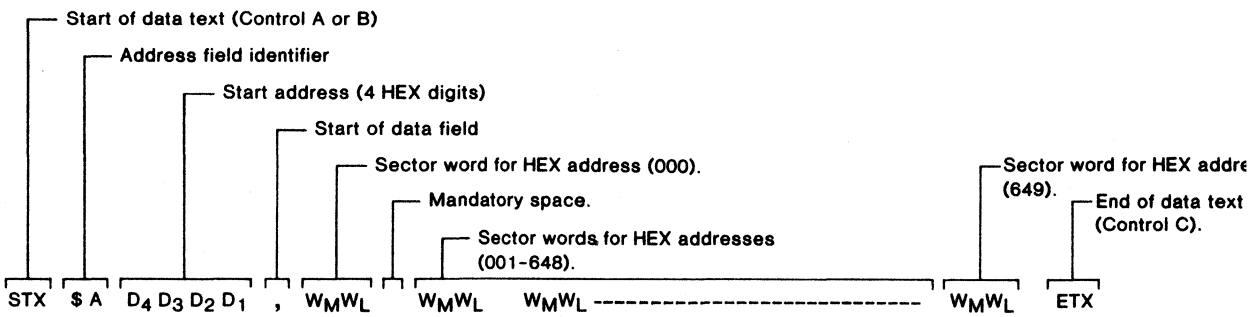
NOTES

1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. T-terms can be re-entered any number of times. The last entry for a particular T-term will be interrupted as valid data.
3. To facilitate an orderly Teletype printout, carriage returns, line feeds, spaces, rubc etc., may be interspersed between data groups, but only preceding an asterisk (
4. Comments are allowed between data fields provided that an asterisk (*) is not use any Heading or Comment entry.

D. Program Table data blocks in MEMORY format are initiated with an STX character, and terminated with an ETX character.

Carriage return and line feed can be interspersed to achieve any preferred teletype printout from tape.

The body of the data consists of address/data information in accordance with the following ASCII-HEX (Space) format. Address fie delimiters may be used to skip over "empty" sector areas:



Entries in the data field are made in groups of 8 bits. These are specified with hexadecimal characters W_MW_L followed by a space t separate sequential address entries. In each 8-bit word W_M specifies the most significant 4 bits and W_L designates the least significant bits.

Other ASCII-HEX formats (Percent, Apostrophe, Comma, etc.) are also acceptable. To insure compatibility with other formats consu Signetics or your programmer manual.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S104/105	0	+75	
	S82S104/105	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S104/105: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S104/105: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S104/105 Min	N82S104/105 Typ[2]	N82S104/105 Max	S82S104/105 Min	S82S104/105 Typ[2]	S82S104/105 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S105)[3,5]	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250		−50	−350	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S105)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S105)[4,8]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	180		120	185	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		10			10		

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{O.E.}$ and a logic high stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{O.E.}$ Output sink current is supplied thru a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{O.E.}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

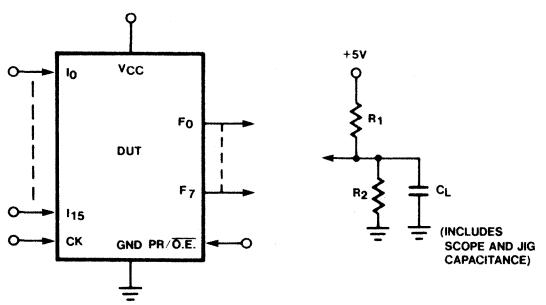
AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S104/105: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S104/105: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

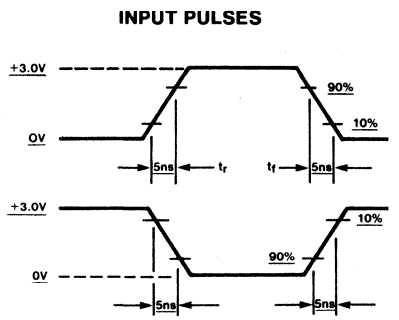
	PARAMETER	TO	FROM	N82S104/105			S82S104/105			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Pulse width									ns
T_{CKH}	Clock[3] high	CK−	CK+	30	15			15		
T_{CKL}	Clock low	CK+	CK−	30	15			15		
T_{CKP}	Period	CK+	CK+	90	65			65		
T_{PRH}	Preset pulse	PR+	PR−	25	15			15		
	Set up time									ns
T_{IS1}	Input	CK+	Input ±	60	40			40		
T_{IS2}	Input (through Complement array)	CK+	Input ±	90	70			70		
T_{VS}	Power-on preset	CK−	V_{CC}+	0	−10			10		
T_{PRS}	Preset	CK−	PR−	0	−10			−10		
	Hold time									ns
T_{IH}	Input	Input ±	CK+		−10	0		−10		
	Propagation delay									ns
T_{CKO}	Clock	Output ±	CK+		25	30		25		
T_{OE}	Output enable	Output−	$\overline{O.E.}$−		20	30		20		
T_{OD}	Output disable	Output+	$\overline{O.E.}$+		20	30		20		
T_{SRE}	State register enable[2]	Output ±	I_O+		50			50		
T_{SRD}	State register disable[2]	Output ±	I_O−		50			50		
T_{PR}	Preset	Output+	PR+		25	35		50		
T_{PPR}	Power-on preset	Output+	V_{CC}+		0	10		0		

NOTE
1. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
2. Diagnostic mode only.
3. To prevent spurious clocking, clock rise time (10%-90%) ≤ 10ns.

TEST LOAD CIRCUIT



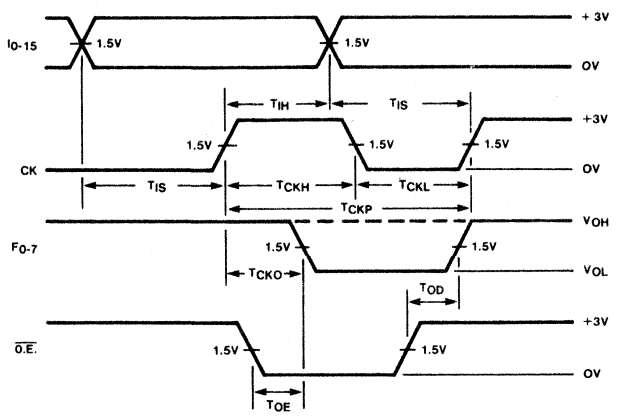
VOLTAGE WAVEFORM



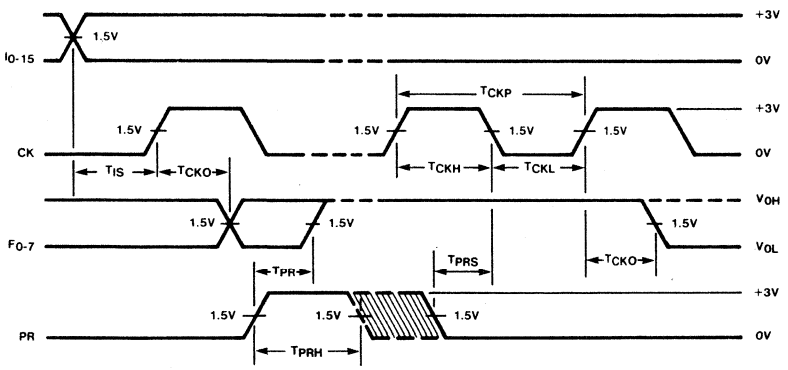
Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

MING DIAGRAMS

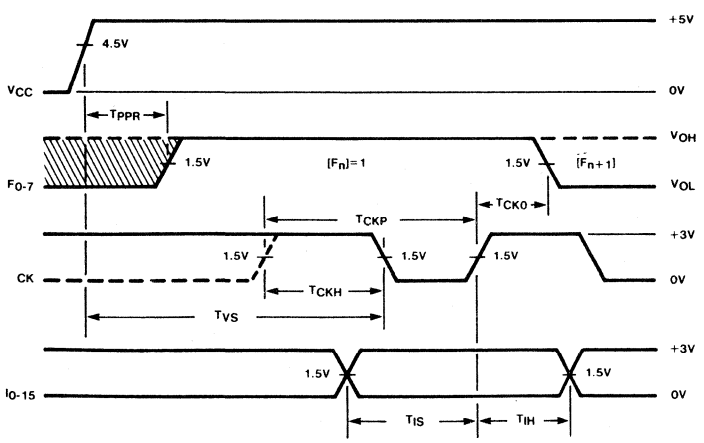
SEQUENTIAL MODE



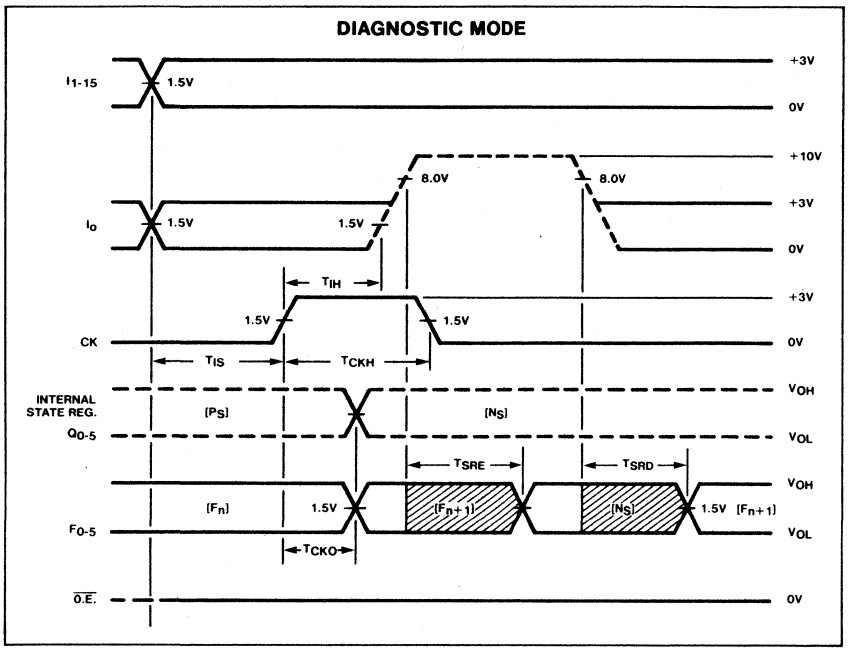
ASYNCHRONOUS PRESET



POWER-ON PRESET



TIMING DIAGRAMS (Cont'd)



MEMORY TIMING DEFINITIONS

T_{CKH} Width of input clock pulse.

T_{CKL} Interval between clock pulses.

T_{CKP} Clock period.

T_{IS1} Required delay between beginning of valid Input and positive transition of clock.

T_{IS2} Required delay between beginning of valid Input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).

T_{VS} Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable cl pulse.

T_{PRS} Required delay between negat transition of asynchronous Pre and negative transition of clock p ceding first reliable clock pulse.

T_{IH} Required delay between posit transition of clock and end of v Input data.

T_{CKO} Delay between positive transitio clock and when Outputs beco valid (with PR/$\overline{O.E.}$ low).

T_{OE} Delay between beginning of Out Enable Low and when Outputs come valid.

T_{OD} Delay between beginning of Out Enable High and when Outputs in the off state.

T_{SRE} Delay between input I_0 transitio Diagnostic mode and when the C puts reflect the contents of State Register.

T_{SRD} Delay between input I_0 transitio Logic mode and when the Outp reflect the contents of the Out Register.

T_{PR} Delay between positive transitio Preset and when Outputs beco valid at "1".

T_{PPR} Delay between V_{CC} (after pow on) and when Outputs beco preset at "1".

T_{PRH} Width of preset input pulse.

BJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

IRGIN STATE[1,2,3]

factory shipped virgin device contains all sible links intact, such that:

PR/$\overline{OE}$ option is set to PR.

All T_n terms are disabled.

All S/R flip-flop inputs are disabled.

Test array is programmed with standard test pattern.

ECOMMENDED PROGRAMMING ROCEDURE

› program the AND, OR, and Complement 'rays in addition to the PR/$\overline{OE}$ option the llowing procedure should be followed. To aximize recovery from programming 'rors, leave all links in unused device areas tact.

ET-UP

ɜrminate all device outputs with a 10kΩ re-stor to V_{CC}. Set GND (pin 14) to 0V.

ROGRAM PR/$\overline{OE}$ OPTION

With PR/$\overline{OE}$ (pin 19) at GND, raise V_{CC} to V_{CCP}.

After t_D delay pulse PR/$\overline{OE}$ to Vix for a duration of tp.

t_D delay after PR/$\overline{OE}$ has returned to GND, lower V_{CC} to V_{CCV} or GND.

ERIFY PR/$\overline{OE}$ OPTION

With PR/$\overline{OE}$ at GND, set V_{CC} to V_{CCV}.

After a delay of t_D raise PR/$\overline{OE}$ to Vix for a minimum duration of T_{RS}.

Return PR/$\overline{OE}$ to GND with a fall time less than T_f.

After t_D delay, pulse PR/$\overline{OE}$ to V_{IH} for a minimum duration of T_{ps}.

After t_D delay, F_O (pin 18) indicates V_{OH} if the PR option is selected and V_{OL} if the $\overline{OE}$ option is programmed.

PROGRAM-VERIFY "AND" ARRAY

1. **SET-UP:**
With V_{CC} at GND and CK at V_{CKV}, select the fuse to be programmed by applying TTL voltage levels to input sets I_{0-5} and I_{7-13} in accordance with the binary address map on page 21. Also set I_{15} = V_{IH}, and I_{14} = V_{IL}. After t_D delay raise V_{CC} to V_{CCP}.

2. **PROGRAM CYCLE:**
After a delay of t_D raise I_{14} to V_{IH}. Proceed after another t_D delay to raise CK to V_{CKP}. Following still another t_D delay, pulse I_{15} to V_{IL} for a duration of t_p. t_D later return CK to V_{CKV}, and then t_D after that return I_{14} to V_{IL}.

3. **VERIFY CYCLE:**
After a t_D delay lower I_{15} to V_{IL} for a duration of t_V. At the end of t_V F_O should indicate a level of V_{OH}; a level of V_{OL} indicates an unsuccessful fusing attempt.

4. **NEXT VARIABLE SELECT (C,Im,Ps) (SAME TERM Tn):**
After t_D delay, apply the next variable select (C,Im,Ps) address to I_{7-13}, then continue with step 2.

5. **NEXT VARIABLE SELECT (C,Im,Ps) (DIFFERENT TERM Tn):**
After t_D, delay apply the next variable select (C,Im,Ps) and term (Tn) addresses to respectively I_{7-13} and I_{0-5}, then continue to step 2.

PROGRAM-VERIFY "OR" ARRAY

1. **SET-UP:**
With V_{CC} at GND and CK at V_{CKV}, select the fuse to be programmed by applying TTL voltage levels to input sets I_{0-5} and I_{7-13} in accordance with the binary address map on page 21. Also set I_{14} = V_{IL}, and I_{15} = V_{IH}. After t_D delay raise V_{CC} to V_{CCP}.

2. **PROGRAM CYCLE:**
After a delay of t_D raise I_{14} to V_{IH}. Proceed after another t_D delay to raise CK to V_{CKP}. Following still another t_D delay pulse I_{15} to V_{IL} for a duration of tp. t_D later return CK to V_{CKV} and then t_D after that return I_{14} to V_{IL}.

3. **VERIFY CYCLE:**
After a t_D delay lower I_{15} to V_{IL} for a duration of t_V. At the end of t_V F_O should indicate a level of V_{OH}; a level of V_{OL} indicates an unsuccessful fusing attempt.

4. **NEXT VARIABLE SELECT (C,Ns,Fn) (SAME TERM (Tn)):**
After t_D delay apply the next variable select (C,Ns,Fn) address to I_{7-13}, then continue with step 2.

5. **NEXT VARIABLE SELECT (C,Ns,Fn) (DIFFERENT TERM (Tn)):**
After t_D delay apply the next variable select (C,Ns,Fn) and term (Tn) addresses to respectively I_{7-13} and I_{0-5}, then continue to step 2.

PROGRAM CYCLE POWER DOWN

When programming of the device is complete, after t_D delay set I_{15} to V_{IH}, I_{14} to V_{IL} and CK to V_{CKV}. After another t_D delay reduce V_{CC} to 0V.

ɔTES

All outputs will be at "1", as preset by initial power-up procedure.
Device can be clocked via test array function.
Test array function MUST be deleted before incorporating user program.

PROGRAM CYCLE ROW/COLUMN FUSE ADDRESSING

VARIABLE SELECT Table[1]

ROW HEX ADDRESS		SELECTED VARIABLE			ROW HEX ADDRESS		SELECTED VARIABLE	
I_{13} I_{12} I_{11}	I_{10} I_9 I_8 I_7				I_{13} I_{12} I_{11}	I_{10} I_9 I_8 I_7		
0	0	OR Array	N_0	SET	4	0	AND Array	I_0
0	1			RESET	4	1		$\overline{I_0}$
0	2		N_1	SET	4	2		I_1
0	3			RESET	4	3		$\overline{I_1}$
0	4		N_2	SET	4	4		I_2
0	5			RESET	4	5		$\overline{I_2}$
0	6		N_3	SET	4	6		I_3
0	7			RESET	4	7		$\overline{I_3}$
0	8		N_4	SET	4	8		I_4
0	9			RESET	4	9		$\overline{I_4}$
0	A		N_5	SET	4	A		I_5
0	B			RESET	4	B		$\overline{I_5}$
0	C		F_0	SET	4	C		I_6
0	D			RESET	4	D		$\overline{I_6}$
0	E		F_1	SET	4	E		I_7
0	F			RESET	4	F		$\overline{I_7}$
1	0		F_2	SET	5	0		I_8
1	1			RESET	5	1		$\overline{I_8}$
1	2		F_3	SET	5	2		I_9
1	3			RESET	5	3		$\overline{I_9}$
1	4		F_4	SET	5	4		I_{10}
1	5			RESET	5	5		$\overline{I_{10}}$
1	6		F_5	SET	5	6		I_{11}
1	7			RESET	5	7		$\overline{I_{11}}$
1	8		F_6	SET	5	8		I_{12}
1	9			RESET	5	9		$\overline{I_{12}}$
1	A		F_7	SET	5	A		I_{13}
1	B			RESET	5	B		$\overline{I_{13}}$
1	C	Complement Array		C	5	C		I_{14}
					5	D		$\overline{I_{14}}$
1	D	Empty Address Space			5	E		I_{15}
↓	↓				5	F		$\overline{I_{15}}$
					6	0		P_0
					6	1		$\overline{P_0}$
					6	2		P_1
					6	3		$\overline{P_1}$
					6	4		P_2
					6	5		$\overline{P_2}$
					6	6		P_3
					6	7		$\overline{P_3}$
					6	8		P_4
					6	9		$\overline{P_4}$
					6	A		P_5
					6	B		$\overline{P_5}$
3	F				6	C	Complement Array	$\overline{C}$

TRANSITION TERM SELECT Table

COLUMN HEX ADDRESS		SELECTED TRANSITION TERM
I_5 I_4	I_3 I_2 I_1 I_0	
0	0	0
0	1	1
0	2	2
0	3	3
0	4	4
0	5	5
0	6	6
0	7	7
0	8	8
0	9	9
0	A	10
0	B	11
0	C	12
0	D	13
0	E	14
0	F	15
1	0	16
1	1	17
1	2	18
1	3	19
1	4	20
1	5	21
1	6	22
1	7	23
1	8	24
1	9	25
1	A	26
1	B	27
1	C	28
1	D	29
1	E	30
1	F	31
2	0	32
2	1	33
2	2	34
2	3	35
2	4	36
2	5	37
2	6	38
2	7	39
2	8	40
2	9	41
2	A	42
2	B	43
2	C	44
2	D	45
2	E	46
2	F	47
3	0	48
3	1	49

NOTES
1. A row address identifies a particular variable coupled to all transition terms.
2. With a variable selected by the row address the column address further selects a coupling fuse for each term.

JECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

OGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
CCP	V_{CC} supply (program)	I_{CCP} = 550mA min	8.25	8.5	8.75	V
CCV	V_{CC} supply (verify)	Transient or steady state	4.75	5.0	5.25	V
CP	I_{CC} limit program	V_{CCP} = +8.50 ± .25V	550		1,000	mA
	Input voltage					V
IH	High		2.4		5.5	
IL	Low		0	0.4	0.8	
	Input Current					μA
H	High	V_{IH} = +5.5V			50	
L	Low	V_{IL} = 0V			−500	
IX	O.E. program enable level		9.5	10	10.5	V
X	O.E. program input current	V_{IX} = +10V			10	mA
CKP	CK supply (program)[3]	I_{CKP} = 300 ± 25mA Transient or steady state	16.0	17.0	18.0	V
CKV	CK supply (idle)	I_{CKV} = 1mA max	1.25	1.5	1.75	V
CKP	CK supply current limit	V_{CKP} = +17 ± 1V	275	300	325	mA
v	Verify time		1			μs
RS	Reset pulse width		1			μs
PS	Preset pulse width		1			μs
p	Programming pulse width		0.3	0.4	0.5	ms
D	Pulse sequence delay		10			μs
R	CK Pulse rise time	10% to 90%	10		50	μs
PVB	Program-Verify time per link			0.6		ms
DC	Programming duty cycle				100	%
L	Fusing attempts per link				2	cycle
S	Verify threshold[4]		1.4	1.5	1.6	V

TES

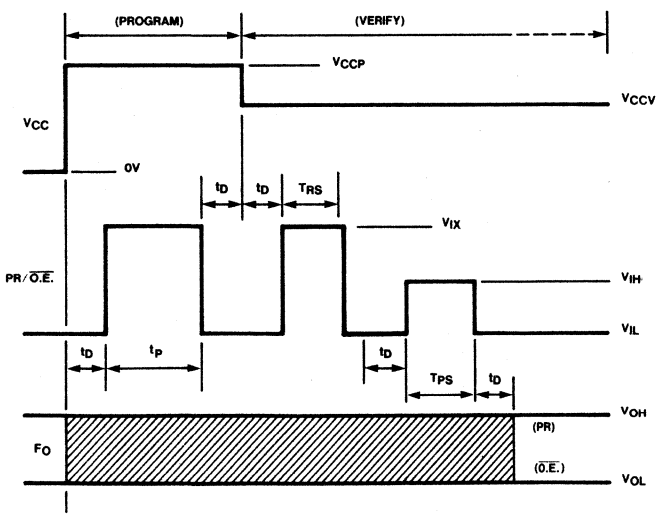
These are specifications which a Programming System must satisfy in order to be qualified by Signetics.

Bypass V_{CC} to GND with a 0.01μf capacitor to reduce voltage spikes.

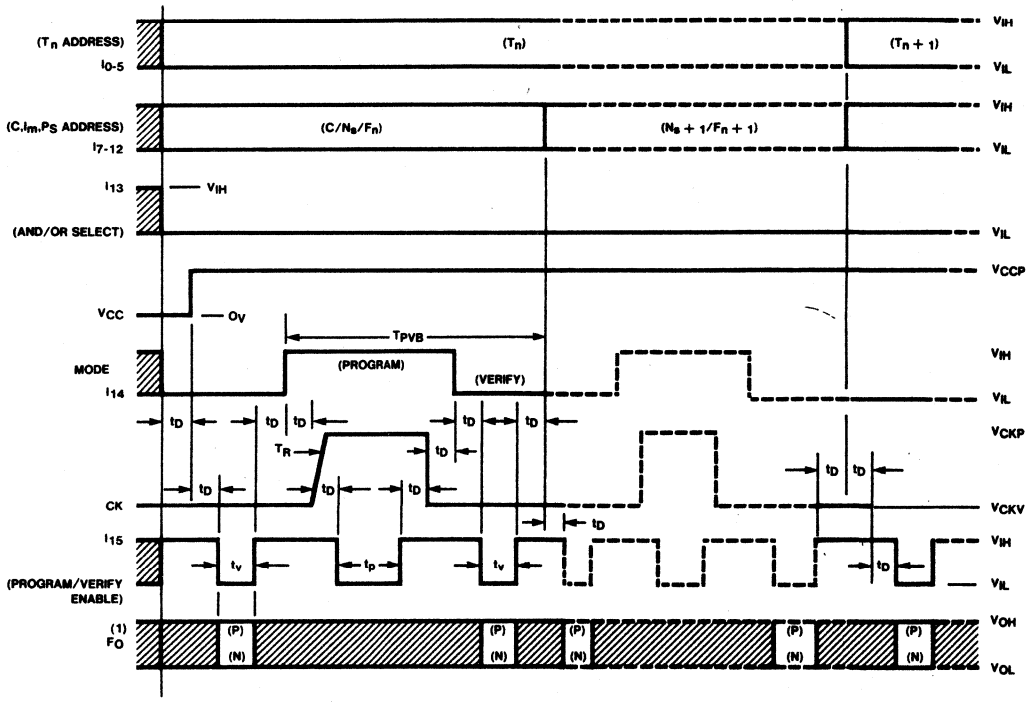
Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

V_S is the sensing threshold of the FPLS output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

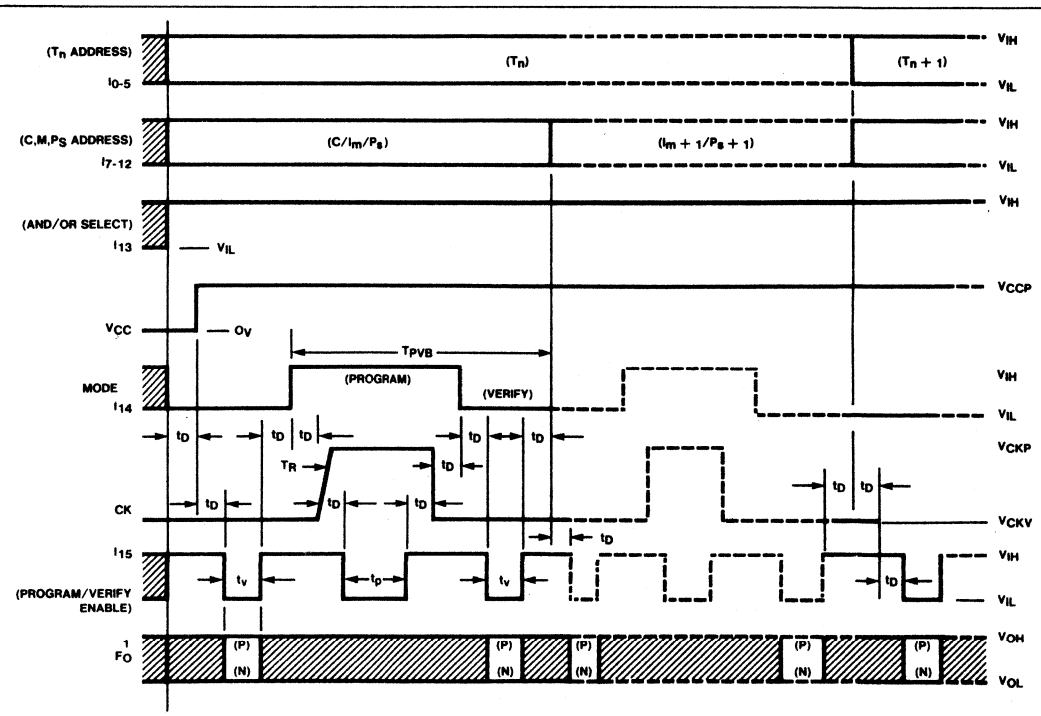
R/O.E. OPTION PROGRAM-VERIFY SEQUENCE



"OR" ARRAY PROGRAM-VERIFY SEQUENCE (TYPICAL)



"AND" ARRAY PROGRAM-VERIFY SEQUENCE (TYPICAL)



NOTE

1. (P) and (N) represent respectively a programmed and non-programmed fuse, corresponding to logic "1" or "0" output voltage levels.

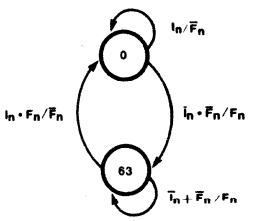
TEST ARRAY

The FPLS may be subjected to AC and DC parametric tests prior to programming via an on chip test array.

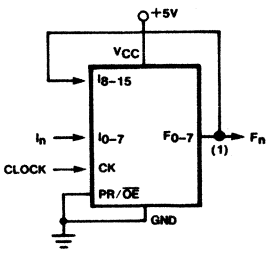
The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-7} as shown in the test circuit timing diagram.

STATE DIAGRAM



FPLS UNDER TEST



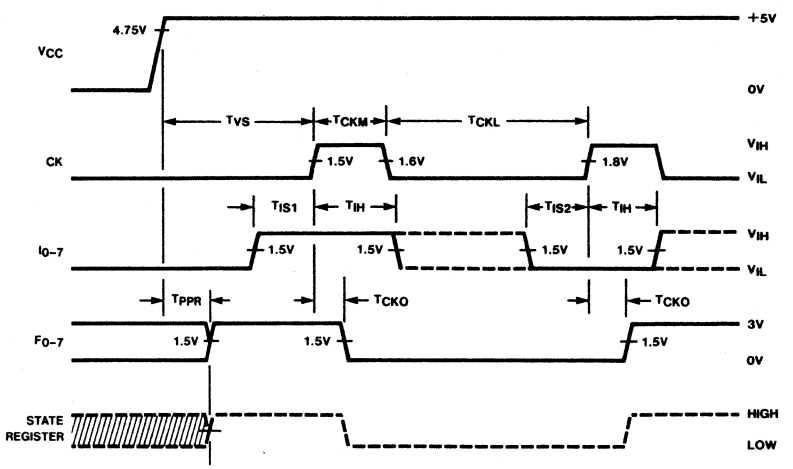
TEST ARRAY PROGRAM (LOGIC)

NO.	C	TRANSITION TERM: INPUT VARIABLE (Im) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PRESENT STATE (Ps) 5	4	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)	H													
OUTPUT TERM														
NEXT STATE (Ns)							OUTPUT FUNCTION (Fn)							
5	4	3	2	1	0	7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetics' qualified programming equipment.

TEST CIRCUIT TIMING DIAGRAM



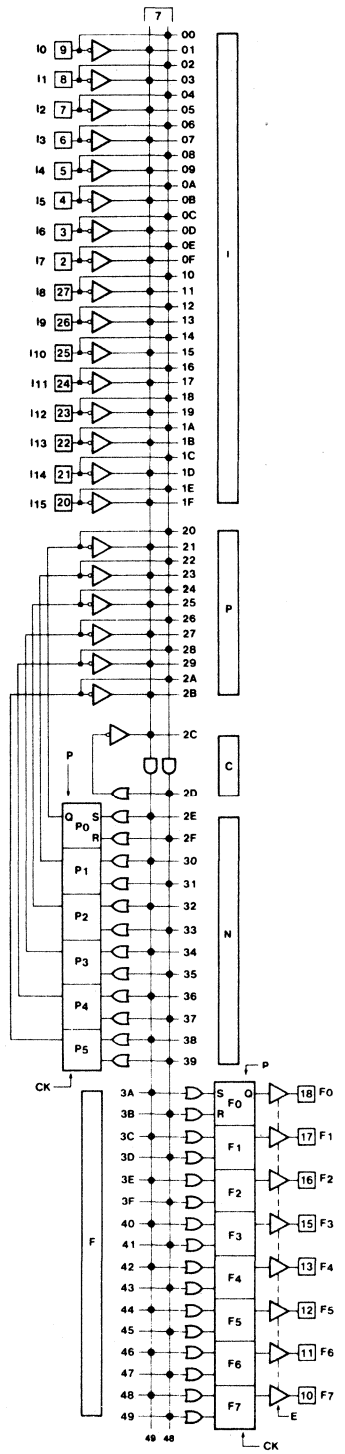
TEST ARRAY DELETED (LOGIC)

NO.	C	TRANSITION TERM: INPUT VARIABLE (Im) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PRESENT STATE (Ps) 5	4	3	2	1	0
48	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)	H													
OUTPUT TERM														
NEXT STATE (Ns)							OUTPUT FUNCTION (Fn)							
5	4	3	2	1	0	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—	—	—

TEST ARRAY PROGRAM (MEMORY)

LOGIC DIAGRAM



TABLE

SECTOR DATA	ADDRESS	V4,5 A R
0:2	700	I_0
0:1	701	
0:2	702	I_1
0:1	703	
0:2	704	I_2
0:1	705	
0:2	706	I_3
0:1	707	
0:2	708	I_4
0:1	709	
0:2	70A	I_5
0:1	70B	
0:2	70C	I_6
0:1	70D	
0:2	70E	I_7
0:1	70F	
0:2	710	I_8
0:1	711	
0:2	712	I_9
0:1	713	
0:2	714	I_{10}
0:1	715	
0:2	716	I_{11}
0:1	717	
0:2	718	I_{12}
0:1	719	
0:2	71A	I_{13}
0:1	71B	
0:2	71C	I_{14}
0:1	71D	
0:2	71E	I_{15}
0:1	71F	
0:2	720	P_0
0:1	721	
0:2	722	P_1
0:1	723	
0:2	724	P_2
0:1	725	

SECTOR DATA	ADDRESS	V4,5 A R
0:2	726	P_3
0:1	727	
0:2	728	P_4
0:1	729	
0:2	72A	P_5
0:1	72B	
0:1	72C	C^6
0:2	72D	
0:1	72E	N_0
0:2	72F	
0:1	730	N_1
0:2	731	
0:1	732	N_2
0:2	733	
0:1	734	N_3
0:2	735	
0:1	736	N_4
0:2	737	
0:1	738	N_5
0:2	739	
0:1	73A	F_0
0:2	73B	
0:1	73C	F_1
0:2	73D	
0:1	73E	F_2
0:2	73F	
0:1	740	F_3
0:2	741	
0:1	742	F_4
0:2	743	
0:1	744	F_5
0:2	745	
0:1	746	F_6
0:2	747	
0:1	748	F_7
0:2	749	

TEST ARRAY DELETED

SECTOR DATA	ADDRESS	V4,5 A R
0:2	700	I_0
0:1	701	
0:2	702	I_1
0:1	703	
0:2	704	I_2
0:1	705	
0:2	706	I_3
0:1	707	
0:2	708	I_4
0:1	709	
0:2	70A	I_5
0:1	70B	
0:2	70C	I_6
0:1	70D	
0:2	70E	I_7
0:1	70F	
0:2	710	I_8
0:1	711	
0:2	712	I_9
0:1	713	
0:2	714	I_{10}
0:1	715	
0:2	716	I_{11}
0:1	717	
0:2	718	I_{12}
0:1	719	
0:2	71A	I_{13}
0:1	71B	
0:2	71C	I_{14}
0:1	71D	
0:2	71E	I_{15}
0:1	71F	
0:2	720	P_0
0:1	721	
0:2	722	P_1
0:1	723	
0:2	724	P_2
0:1	725	

SECTOR DATA	ADDRESS	V4,5 A R
0:2	726	P_3
0:1	727	
0:2	728	P_4
0:1	729	
0:2	72A	P_5
0:1	72B	
0:1	72C	C^6
0:3	72D	
0:3	72E	N_0
0:3	72F	
0:3	730	N_1
0:3	731	
0:3	732	N_2
0:3	733	
0:3	734	N_3
0:3	735	
0:3	736	N_4
0:3	737	
0:3	738	N_5
0:3	739	
0:3	73A	F_0
0:3	73B	
0:3	73C	F_1
0:3	73D	
0:3	73E	F_2
0:3	73F	
0:3	740	F_3
0:3	741	
0:3	742	F_4
0:3	743	
0:3	744	F_5
0:3	745	
0:3	746	F_6
0:3	747	
0:3	748	F_7
0:3	749	

For memory type programmers, test arra
terms 48 and 49 have been mapped as th
two least significant terms in the LOW grou
of Sector 7.

Note that addresses 74A to 7FF represer
"empty" locations for which the only lega
data is "0".

Since Sector 7 contains just 2 terms, th
most significant digit of Sector Data is "0"
and the least significant can only range fro
"0" to "3".

BJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

ESCRIPTION

e 82S106 (Open collector outputs) and 3107 (3-state outputs) are bipolar Pro-mmable ROM Patches organized as 48 rds by 8 bits, addressed via a 16 bit grammable address comparator. Each rd can be assigned a unique address de, P_n, within a 64K (2^{16}) address range by gramming the comparator inputs High, w, or Don't care via True/Complement ut buffers.

e contents of each word are also pro-mmable, and are enabled to the active-gh Patch outputs only when a pro-mmed address is detected, which causes $\overline{\text{Flag}}$ output to go Low. For all unpro-mmed addresses, the device outputs ain High (82S106) or Hi-Z (82S107) while $\overline{\text{Flag}}$ output remains High. The $\overline{\text{Flag}}$ is en collector to allow wire-ANDing for ansion to more than 48 patch words.

e 82S106 and 82S107 are fully TTL com-ible and can be programmed in the field following the fusing procedure outlined his data sheet, or by means of commer-lly available equipment.

th devices are available in commercial d military temperature ranges. For the mmercial range (0°C to +75°C) specify 2S106/107, F or N, and for the military nperature range (-55°C to +125°C) spec-S82S106/107, F, G, or R.

FEATURES

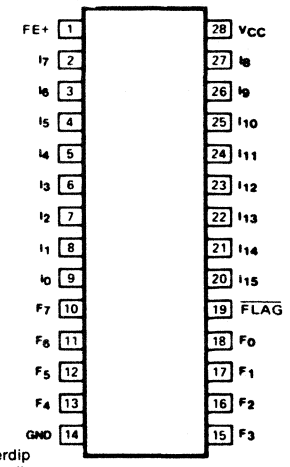
- **Field programmable (Ni-Cr link)**
- **Address Inputs: 16**
- **Data Outputs: 8**
- **Patch Words: 48**
- **Address access time:**
  S82S106/107—100ns Max
  N82S106/107—70ns Max
- **Power dissipation: 600mW typ**
- **Input loading:**
  S82S106/107: -150μA Max
  N82S106/107: -100μA Max
- **Open collector $\overline{\text{Flag}}$**
- **Output option:**
  82S106: Open collector
  82S107: 3-state
- **Output disabled state**
  3-state—Hi-Z
  Open collector—Hi

APPLICATIONS

- **ROM data modifications**
- **Memory address trap**
- **Digital filter**
- **Interrupt request/vector generator**
- **Data security encoder**

PIN CONFIGURATION

F,G,I,N.R PACKAGE*

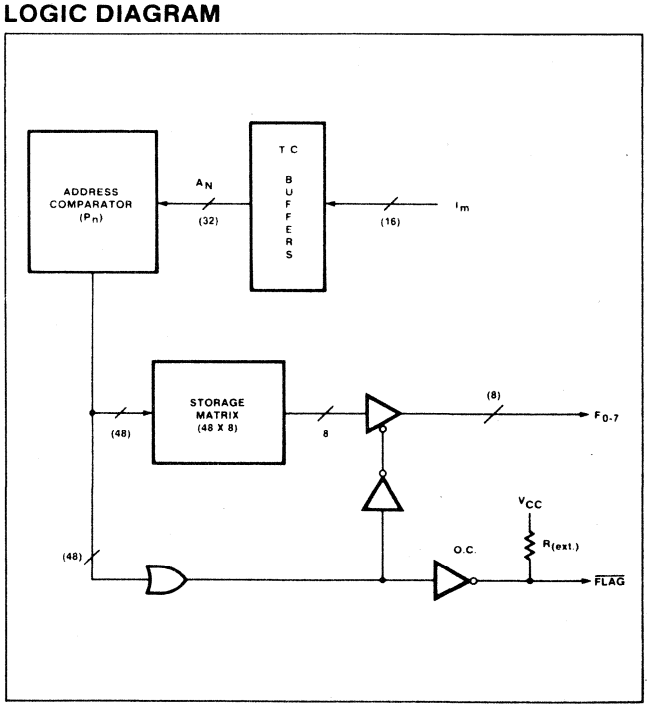


F = Cerdip
G = Leadless
*I = Ceramic
N = Plastic
R = Flat pack
†Open or grounded during normal operation

TRUTH TABLE

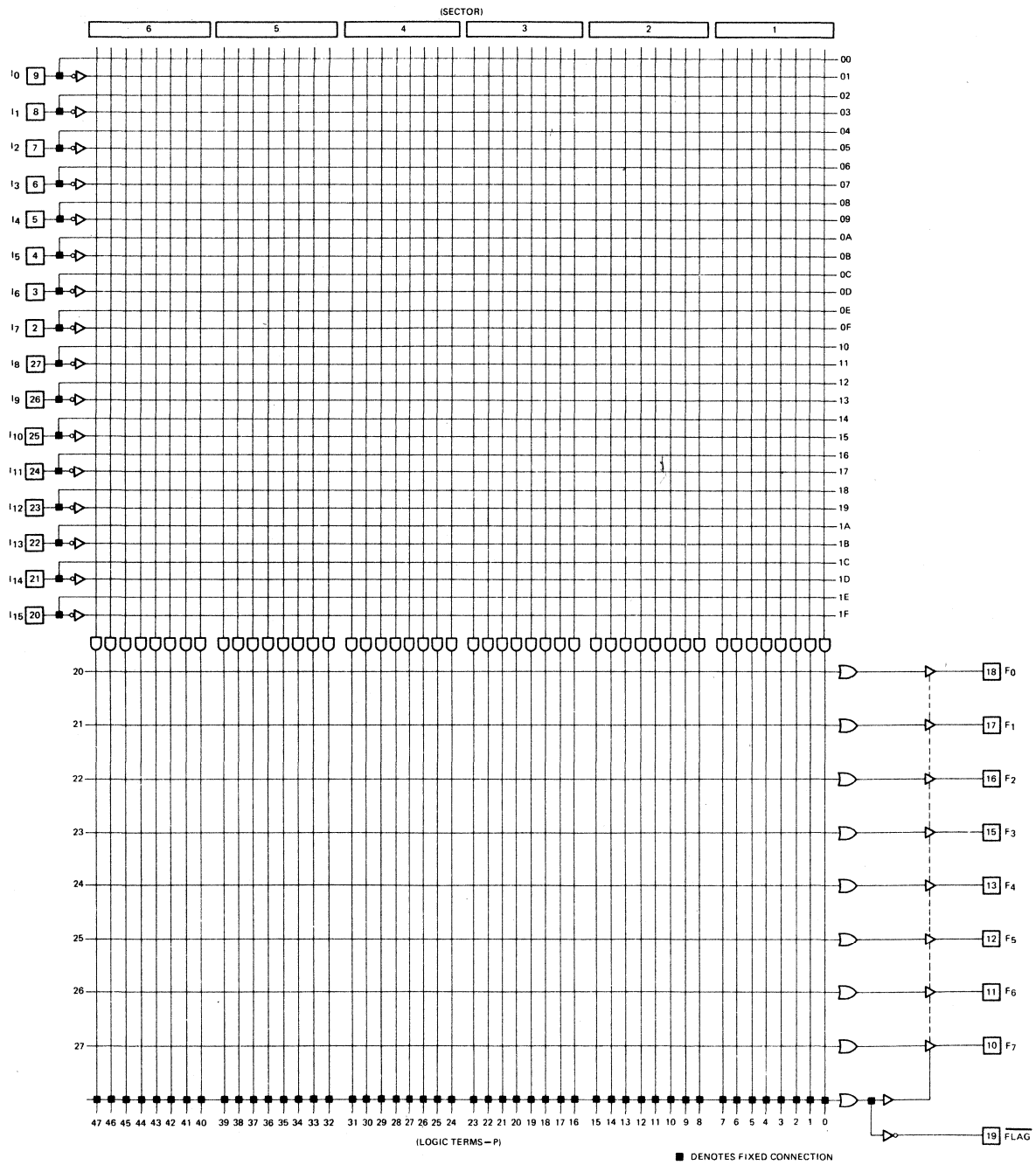
$A_N \stackrel{?}{=} P_N$	$\overline{\text{Flag}}$	F_{0-7}	
		82S106	82S107
NO	1	1	Hi-Z
YES	0	Stored Data	

LOGIC DIAGRAM



BIPOLAR MEMORY

FPRP LOGIC DIAGRAM



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S106/107	0	+75	
	S82S106/107	-55	+125	
T_{STG}	Storage	-65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S106/107: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S106/107: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S106/107 Min	N82S106/107 Typ[2]	N82S106/107 Max	S82S106/107 Min	S82S106/107 Typ[2]	S82S106/107 Max	UNIT
	Input voltage[2]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp [2,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S107)[2,4]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[2,5] (F_{0-7})	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OL}	Low[2,5] ($\overline{Flag}$)	I_{OL} = 4.8mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S107)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S107)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[6]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S106/107: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S106/107: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S106/107 Min	N82S106/107 Typ	N82S106/107 Max	S82S106/107 Min	S82S106/107 Typ	S82S106/107 Max	UNIT
	Access time									ns
T_{IA}	Address	Output	Input		45	70		100	100	
T_{FL}	Enable	$\overline{Flag}$	Input		40	55		40	80	

NOTES on following page.

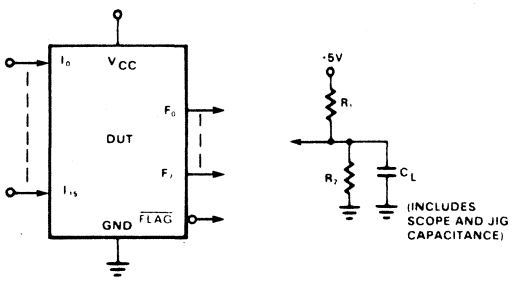
OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

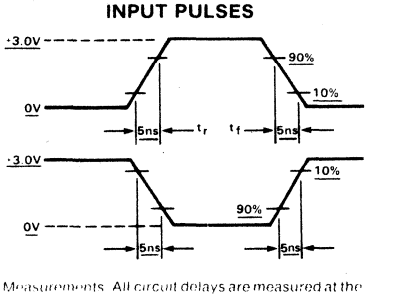
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specification is not implied.
2. **All typical values are at V_{CC} = 5V, T_A = 25°C.**
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with the Patch enabled (A_N - P_N) and a logic high stored.
6. Measured with a programmed logic condition for which the output under test is at low logic level when the Patch is enabled (A_N - P_N). Output sink current is applied thr a resistor to V_{CC}.
7. Measured with the Patch disabled (A_N ≠ P_N).
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with all inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

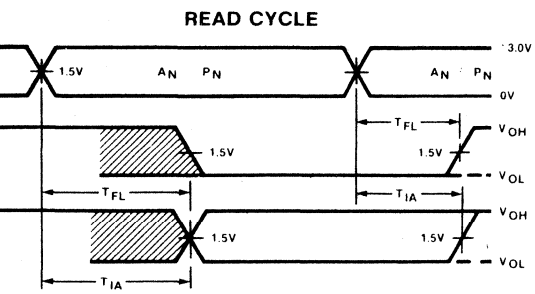


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{IA} Delay between latest Address variable change and when Data Output becomes stable.

T_{FL} Delay between latest Address variable change and when Flag output becomes stable.

VIRGIN DEVICE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "false").
3. The "OR" Matrix contains all 48-P-terms.
4. The polarity of each output is set to active high (Fp function).
5. All outputs are at a low logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the "AND" matrix, "OR" matrix, and output polarity outlined below. To maximize recovery from programming errors, leave all links in unused device areas intact.

SET-UP

Terminate all device outputs with a 10K resistor to +5V. Set GND (pin 14) to 0V.

ADDRESS COMPARATOR

Program Pn Address

Program one input at the time and one P-term at the time. Unused comparator inputs must be programmed as Don't Care for all programmed P-terms.

1. Set FE (pin 1) to V_{FEL}, and V_{CC} (pin 28) to V_{CCP}.
2. Disable all device outputs by setting $\overline{Flag}$ (pin 19) to V_{IH}.
3. Disable all comparator inputs by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.
5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.
5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step 6.
5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step 6.
6a. After t_D delay, raise FE from V_{FEL} to V_{FEH}.
6b. After t_D delay, pulse the $\overline{Flag}$ input from V_{IH} to V_{IX} for a period t_p.
6c. After t_D delay, return FE input to V_{FEL}.
7. Disable programmed input by returning I_0 to V_{IX}.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove V_{IX} from all input variables.

VERIFY P_n ADDRESS

1. Set FE to V_{FEL}, and V_{CC} to V_{CCP}.
2. Enable F_7 output by setting $\overline{Flag}$ to V_{IX}.
3. Disable all comparator inputs by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.
5. Interrogate Input I_0 as follows:
   A. Lower the input voltage at I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.
   B. Lower the input voltage at I_0 from V_{IH} to V_{IL}, and sense the logic state output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	COMPARATOR INPUT STATE CONTAINED IN P-TERM
0	1	$\overline{I_0}$
1	0	
0	0	I_0
1	1	
0	1	Don't Care
1	1	
0	0	(I_0), ($\overline{I_0}$)
1	0	

Note that 2 tests are required to uniquely determine the state of the input contained in the P-term.

6. Disable verified input by returning I_0 to V_{IX}.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{IX} from all comparator inputs.

STORAGE MATRIX

Program Output Data

Program one output at the time for one P-term at the time.

1. Set FE to V_{FEL}.
2. Disable the chip by setting $\overline{Flag}$ to V_{IH}.
3. After t_D delay, set V_{CC} to V_{CCS}, and inputs I_6 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to comparator inputs I_0 through I_5, with I_0 as LSB.
5. To program a logic "0" at output F_0, force F_0 to V_{OPF}.
6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.
6b. After t_D delay, pulse the $\overline{Flag}$ input from V_{IH} to V_{IX} for a period t_p.
6c. After t_D delay, return FE input to V_{FEL}.
6d. After t_D delay, remove V_{OPF} from output F_0.
7. Repeat steps 5 and 6 for all other output functions.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{CCS} from V_{CC}.

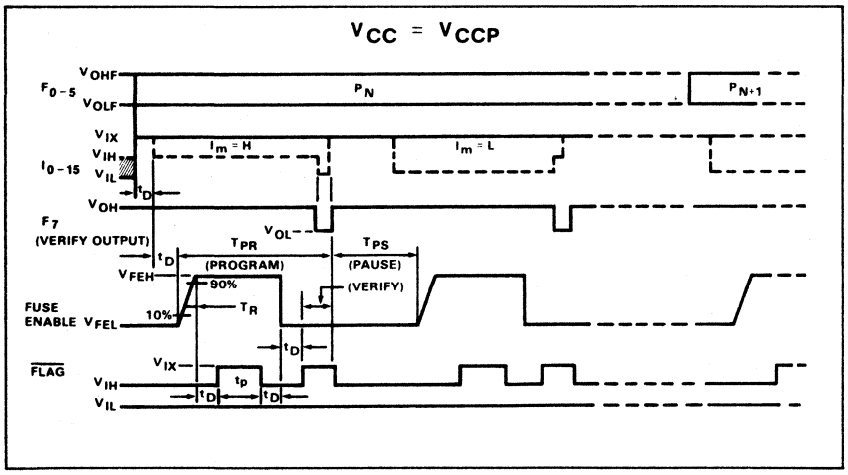
Verify Output Data

1. Set FE to V_{FEL}.
2. Disable the chip by setting $\overline{Flag}$ to V_{IH}.
3. After t_D delay, set V_{CC} to V_{CCS}, and inputs I_0 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to comparator inputs I_0 through I_5.
5. After t_D delay, enable the chip by setting $\overline{Flag}$ to V_{IL}.
6. To determine the status of each output link in the Storage Matrix, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

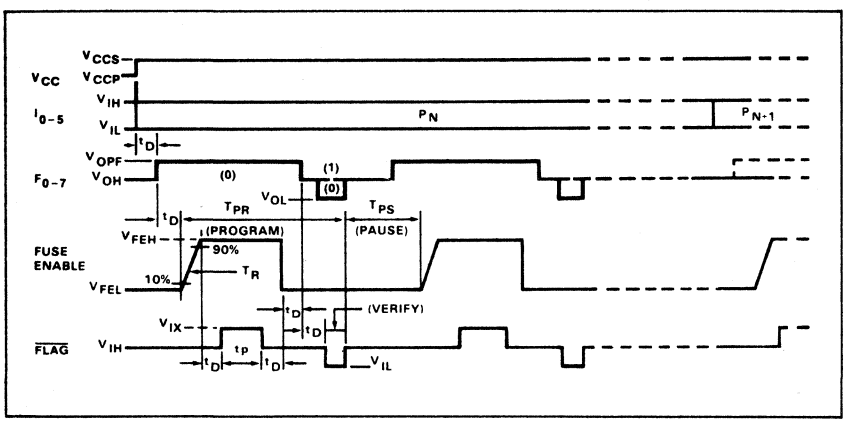
F_P	LINK
0	Fused
1	Present

7. Repeat steps 4 through 6 for all other P-terms.
8. Remove V_{CCS} from V_{CC}.

ADDRESS COMPARATOR PROGRAM-VERIFY SEQUENCE (TYPICAL)



STORAGE MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

PROGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCS}	V_{CC} supply (program/verify Storage Matrix)[2]	I_{CCS} = 550mA, min. Transient or steady state	8.25	8.5	8.75	V
I_{CCS}	I_{CC} limit	V_{CCS} = +8.50 ± .25V	550		1,000	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
	Forced output voltage					V
V_{OHF}	High		2.4		5.5	
V_{OLF}	Low		0	0.4	0.8	
	Output current					
I_{OHF}	High	V_{OHF} = +5.5V			100	μA
I_{OLF}	Low	V_{OLF} = 0V			-1	mA
V_{IX}	$\overline{\text{Flag}}$ program enable level		9.5	10	10.5	V
I_{IX1}	$\overline{\text{Flag}}$ input current	V_{IX} = +10V			10	mA
I_{IX2}	$\overline{\text{Flag}}$ input current	V_{IX} = +10V			10	mA
V_{FEH}	FE supply (program)[3]	I_{FEH} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
V_{FEL}	FE supply (idle)	I_{FEL} = -1mA, max	1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = +17 ± 1V	275	300	325	mA
V_{CCP}	V_{CC} supply (program/verify Address Comparator)	I_{CCP} = 550mA, min. Transient or steady state	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit	V_{CCP} = +5.0 ± .25V	550		1,000	mA
V_{OPF}	Forced output (program)		9.5	10	10.5	V
I_{OPF}	Output current (program)				10	mA
T_R	FE pulse rise time	10% to 90%	10		50	μs
t_P	$\overline{\text{Flag}}$ programming pulse width		0.3	0.4	0.5	ms[5]
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR} + T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

These are specifications which a Programming System must satisfy in order to be qualified by Signetics.

Bypass V_{CC} to GND with a 0.01μf capacitor to reduce voltage spikes.

Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

4. V_S is the sensing threshold of the FPRP output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
5. These are new limits resulting from device improvements, and which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

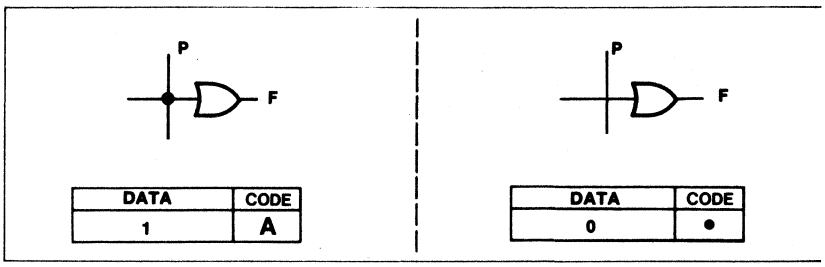
LOGIC PROGRAMMING

The FPRP can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from memory patch specifications using the Program Table on the following page.

In this Table, the logic state of variables I and F associated with each Patch address P_n is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

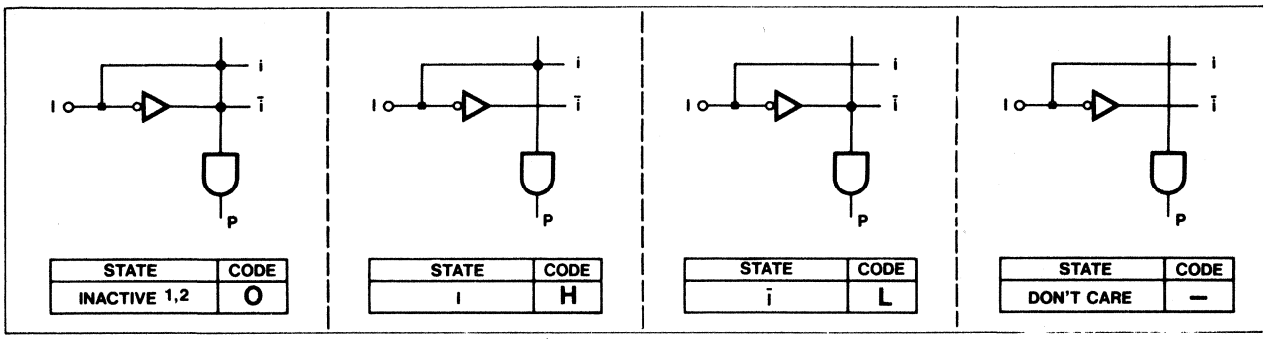
"OR" ARRAY - (F)



DATA	CODE
1	A

DATA	CODE
0	•

"AND" ARRAY - (I),



STATE	CODE
INACTIVE [1,2]	O

STATE	CODE
I	H

STATE	CODE
$\bar{I}$	L

STATE	CODE
DON'T CARE	–

NOTES
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

FPRP PROGRAM TABLE (Logic)

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) ______

CUSTOMER SYMBOLIZED PART # ______

DATE RECEIVED ______

COMMENTS ______

CUSTOMER NAME ______

PURCHASE ORDER # ______

SIGNETICS DEVICE # ______

TOTAL NUMBER OF PARTS ______

PROGRAM TABLE # ______

REV ______ DATE ______

PROGRAM TABLE ENTRIES				
COMPARATOR INPUT			OUTPUT FUNCTION	
I_m	$\overline{I_m}$	Don't care	"1"	"0"
H	L	— (dash)	A	• (period)

NOTES
1. Enter (-) for unused inputs of all active P-terms.
2. Enter (A) for unused outputs of all active P-terms.
3. Unused inputs and outputs are FPRP terminals left floating.
4. Input and output fields of inactive P-terms can be left blank.

PRODUCT TERM																	ACTIVE LEVEL							
	INPUT VARIABLE																H	H	H	H	H	H	H	H
																	OUTPUT FUNCTION							
NO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
4																								
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OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 28

FPRP PROGRAM TABLE (Memory)[1,2]

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV _____ DATE _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	SECTOR DATA	ADDRESS	VAR[3,4]
:	600	:	500	:	400	:	300	:	200	:	100	I_0
:	601	:	501	:	401	:	301	:	201	:	101	
:	602	:	502	:	402	:	302	:	202	:	102	I_1
:	603	:	503	:	403	:	303	:	203	:	103	
:	604	:	504	:	404	:	304	:	204	:	104	I_2
:	605	:	505	:	405	:	305	:	205	:	105	
:	606	:	506	:	406	:	306	:	206	:	106	I_3
:	607	:	507	:	407	:	307	:	207	:	107	
:	608	:	508	:	408	:	308	:	208	:	108	I_4
:	609	:	509	:	409	:	309	:	209	:	109	
:	60A	:	50A	:	40A	:	30A	:	20A	:	10A	I_5
:	60B	:	50B	:	40B	:	30B	:	20B	:	10B	
:	60C	:	50C	:	40C	:	30C	:	20C	:	10C	I_6
:	60D	:	50D	:	40D	:	30D	:	20D	:	10D	
:	60E	:	50E	:	40E	:	30E	:	20E	:	10E	I_7
:	60F	:	50F	:	40F	:	30F	:	20F	:	10F	
:	610	:	510	:	410	:	310	:	210	:	110	I_8
:	611	:	511	:	411	:	311	:	211	:	111	
:	612	:	512	:	412	:	312	:	212	:	112	I_9
:	613	:	513	:	413	:	313	:	213	:	113	
:	614	:	514	:	414	:	314	:	214	:	114	I_{10}
:	615	:	515	:	415	:	315	:	215	:	115	
:	616	:	516	:	416	:	316	:	216	:	116	I_{11}
:	617	:	517	:	417	:	317	:	217	:	117	
:	618	:	518	:	418	:	318	:	218	:	118	I_{12}
:	619	:	519	:	419	:	319	:	219	:	119	
:	61A	:	51A	:	41A	:	31A	:	21A	:	11A	I_{13}
:	61B	:	51B	:	41B	:	31B	:	21B	:	11B	
:	61C	:	51C	:	41C	:	31C	:	21C	:	11C	I_{14}
:	61D	:	51D	:	41D	:	31D	:	21D	:	11D	
:	61E	:	51E	:	41E	:	31E	:	21E	:	11E	I_{15}
:	61F	:	51F	:	41F	:	31F	:	21F	:	11F	
:	620	:	520	:	420	:	320	:	220	:	120	F_0
:	621	:	521	:	421	:	321	:	221	:	121	F_1
:	622	:	522	:	422	:	322	:	222	:	122	F_2
:	623	:	523	:	423	:	323	:	223	:	123	F_3
:	624	:	524	:	424	:	324	:	224	:	124	F_4
:	625	:	525	:	425	:	325	:	225	:	125	F_5
:	626	:	526	:	426	:	326	:	226	:	126	F_6
:	627	:	527	:	427	:	327	:	227	:	127	F_7

NOTES:

1. All HEX addresses denote programmable links at Row-Sector locations as shown on the FPRP logic diagram. Sector data specifies the programmed state of fusible links coupling the indicated variable to designated sets of terms. These are sectioned from left to right in HIGH and LOW groups of 4, to which HEX data is assigned in accordance with the definitions below. The LOW group corresponds to least significant HEX digit.
2. Since memory programmers display a continuous address field, 7 "empty" address fields exist between program table sectors, such as (000-0FF), (128-1FF), (228-2FF), etc. The only entry allowed in these fields is "00".
3. Even row addresses in the AND array correspond to links I.
4. Odd row addresses in the AND array correspond to links $\bar{I}$.

TYPICAL TABLE ENTRY

SECTOR DATA	ADDRESS	VAR
5 : A	1 00	I_0

- I_0 — PROGRAMMED VARIABLE.
- 00 — ROW ADDRESS. (00) SELECTS VARIABLE I_0.
- 1 — SECTOR ADDRESS. (1) SELECTS TERMS 7–0.
- A — (LSD) HEX CHARACTER DENOTING PROGRAMMED CONNECTIONS FROM I_0 TO TERMS 3–0.
- 5 — HEX CHARACTER DENOTING PROGRAMMED CONNECTIONS FROM I_0 TO TERMS 7–4.

MEMORY PROGRAMMING

The FPRP can also be programmed with Memory programming equipment, in conjunction with the FPRP logic diagram. With Memory programming, all links at the AND and OR array cross-points are treated as memory locations with row-sector addresses. Rows are consecutively scanned while each sector addresses eight Product Terms P_n simultaneously. All necessary gate connections are first translated from the Address Patch table as "dot" connections at appropriate locations on the logic diagram. The "dot" connection pattern is then transferred to the corresponding Variable-Address locations on the Program Table using (0) = "dot", (1) = blank in a HEX format:

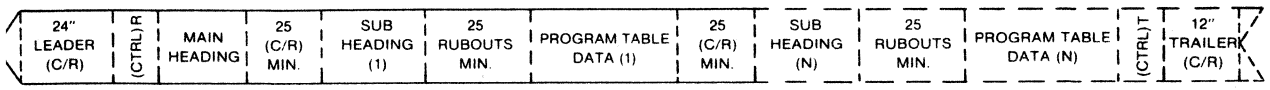
PROGRAMMING DEFINITIONS

LINK	STATUS	CODE
⊕ or ✳	CLOSED	0
┼	OPEN	1

WX TAPE CODING FORMAT

ıe FPRP Program Table can be sent to gnetics in ASCII code format via airmail ;ing any type of 8-level tape (paper, mylar; nfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



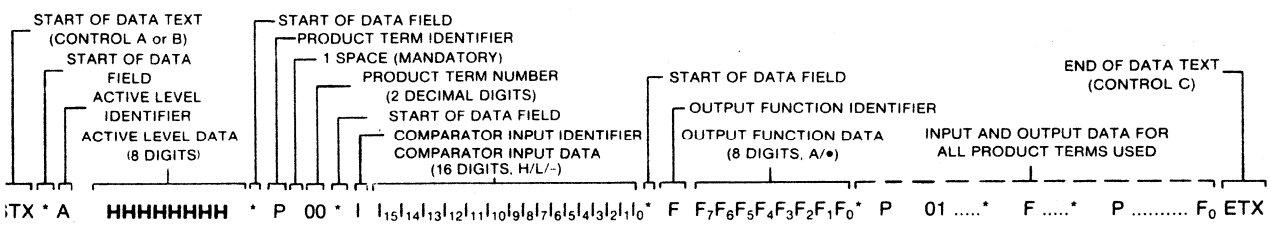
\. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

i. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

:. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



COMPARATOR INPUT		
I_m	$\overline{I_m}$	Don't care
H	L	—(dash)

OUTPUT FUNCTION	
"1"	"0"
A	• (period)

NOTES
1. Enter (-) for unused inputs of all active P-terms.
2. Enter (A) for unused outputs of all active P-terms.
3. Unused inputs and outputs are FPRP terminals left floating.

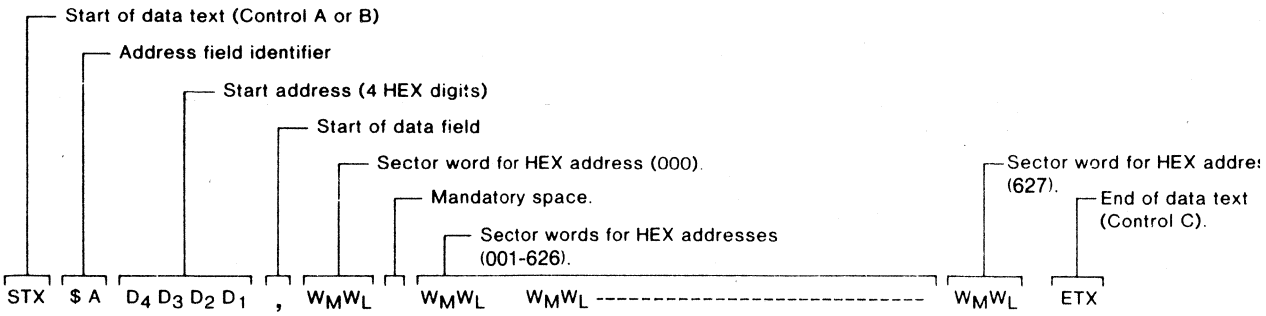
lthough the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if esired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of roduct Terms entered.

OTES
Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk(*).
Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

D. Program Table data blocks in MEMORY format are initiated with an STX character, and terminated with an ETX character.

Carriage return and line feed can be interspersed to achieve any preferred teletype printout from tape.

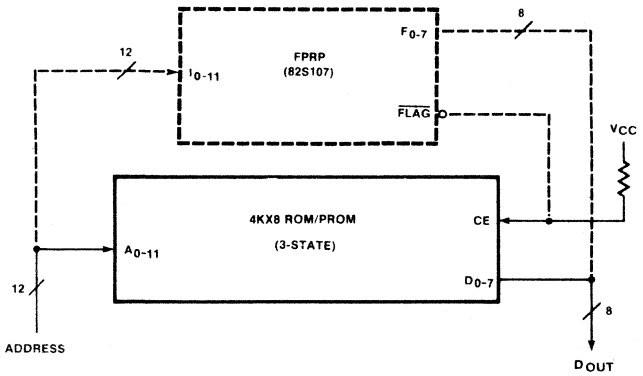
The body of the data consists of address/data information in accordance with the following ASCII-HEX (Space) format. Address fiel delimiters may be used to skip over "empty" sector areas:



Entries in the data field are made in groups of 8 bits. These are specified with hexadecimal characters W_MW_L followed by a space t separate sequential address entries. In each 8-bit word W_M specifies the most significant 4 bits and W_L designates the least significant bits.

Other ASCII-HEX formats (Percent, Apostrophe, Comma, etc.) are also acceptable. To insure compatibility with other formats consul Signetics or your programmer manual.

TYPICAL APPLICATION



PATCH SPECIFICATIONS

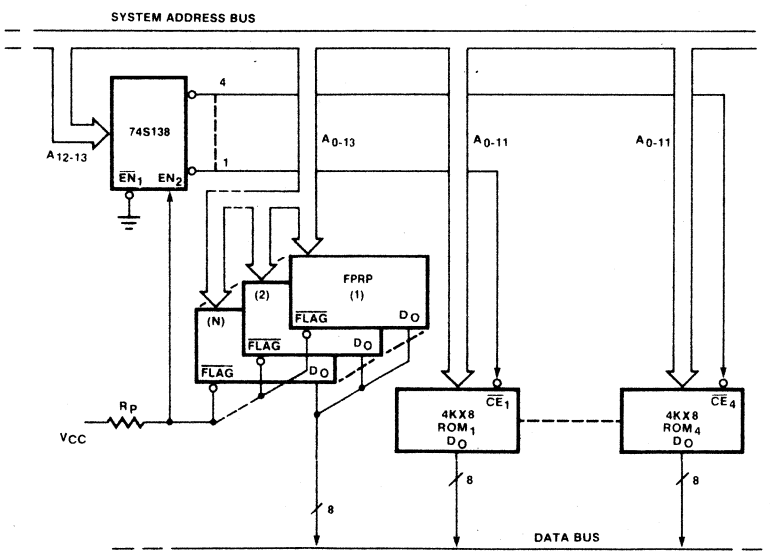
ADDRESS	NEW DATA
750	A9
5FE	7F
0A4	B4
0A5	
0A6	
0A7	

FPRP PROGRAM TABLE

INPUT ADDRESS	PRODUCT TERM NO.	COMPARATOR INPUT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ACTIVE LEVEL H H H H H H H H OUTPUT FUNCTION 7	6	5	4	3	2	1	0	OUTPUT DATA
750	0	–	–	–	–	L	H	H	H	L	H	L	H	L	L	L	L	A	•	A	•	A	•	•	A	A9
5FE	1	–	–	–	–	L	H	L	H	H	H	H	H	H	H	H	L	•	A	A	A	A	A	A	A	7F
0A4·0A7	2	–	–	–	–	L	L	L	L	H	L	H	L	L	H	–	–	A	•	A	A	•	A	•	•	B4
I/O ASSIGNMENT		UNUSED				A_{11}											A_0	D_7							D_0	

Since Patch inputs I_{12-15} are unused, they are programmed Don't Care (–), and left open in the circuit. Note however that I_0 and I_1 are programmed as (–) in P-term 2 because they define an address block of 4 memory locations.

EXPANSION



When more than 48 memory locations need to be patched, several devices can be paralleled by wire-ANDing the $\overline{Flag}$ outputs.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S150 and the 82S151 are single level logic elements, consisting of 12 AND gates with fusible link connections for programming I/O polarity, I/O direction and output enable control.

All gates are linked to 6 inputs (I) and 12 bidirectional I/O lines (B). These yield variable I/O gate configurations via 3 direction control gates (D), ranging from 18 inputs to 12 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to each AND gate. The polarity of all gate outputs is individually programmable through a set of EX-OR gates for implementing AND/NAND logic functions. Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its inputs and output (DeMorgan's Theorem).

The 82S150 and the 82S151 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Both devices are available in a 20-pin slim line package. For the commercial temperature range (0°C to +75°C) specify N82S150/151 N or F. For the military temperature range (−55°C to +125°C) specify S82S150/151 F only.

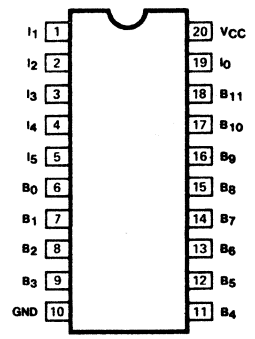
FEATURES

- **Field Programmable (Ni-Cr link)**
- **6 inputs**
- **12 AND gates**
- **12 bidirectional I/O lines**
- **Active high or low outputs**
- **Programmable output enable**
- **Power dissipation: 650mW (typ)**
- **I/O propagation delay: 30ns (max)**
- **Input loading**
  N82S150/151: −100μA (max)
  S82S150/151: −150μA (max)
- **Output options**
  82S150: open collector
  82S151: tri-state
- **TTL compatible**

APPLICATIONS

- **Random gating functions**
- **Address decoding**
- **Code detectors**
- **Memory mapped I/O**
- **Fault monitors**
- **I/O port decoders**

PIN CONFIGURATION



F = Ceramic
N = Plastic

LOGIC FUNCTIONS

Typical Gate Functions:

At L = Open

$X = A \bullet \overline{B} \bullet C \bullet \ldots\ldots$

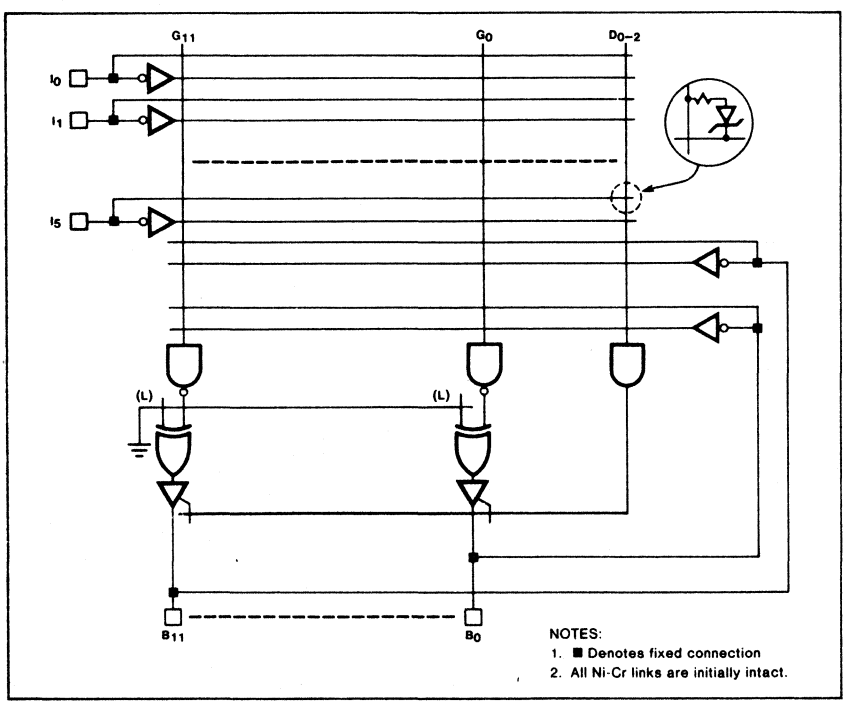
At L = Closed

$X = \overline{A} \bullet \overline{B} \bullet C \bullet \ldots\ldots$

$X = \overline{A} + B + \overline{C} + \ldots\ldots$

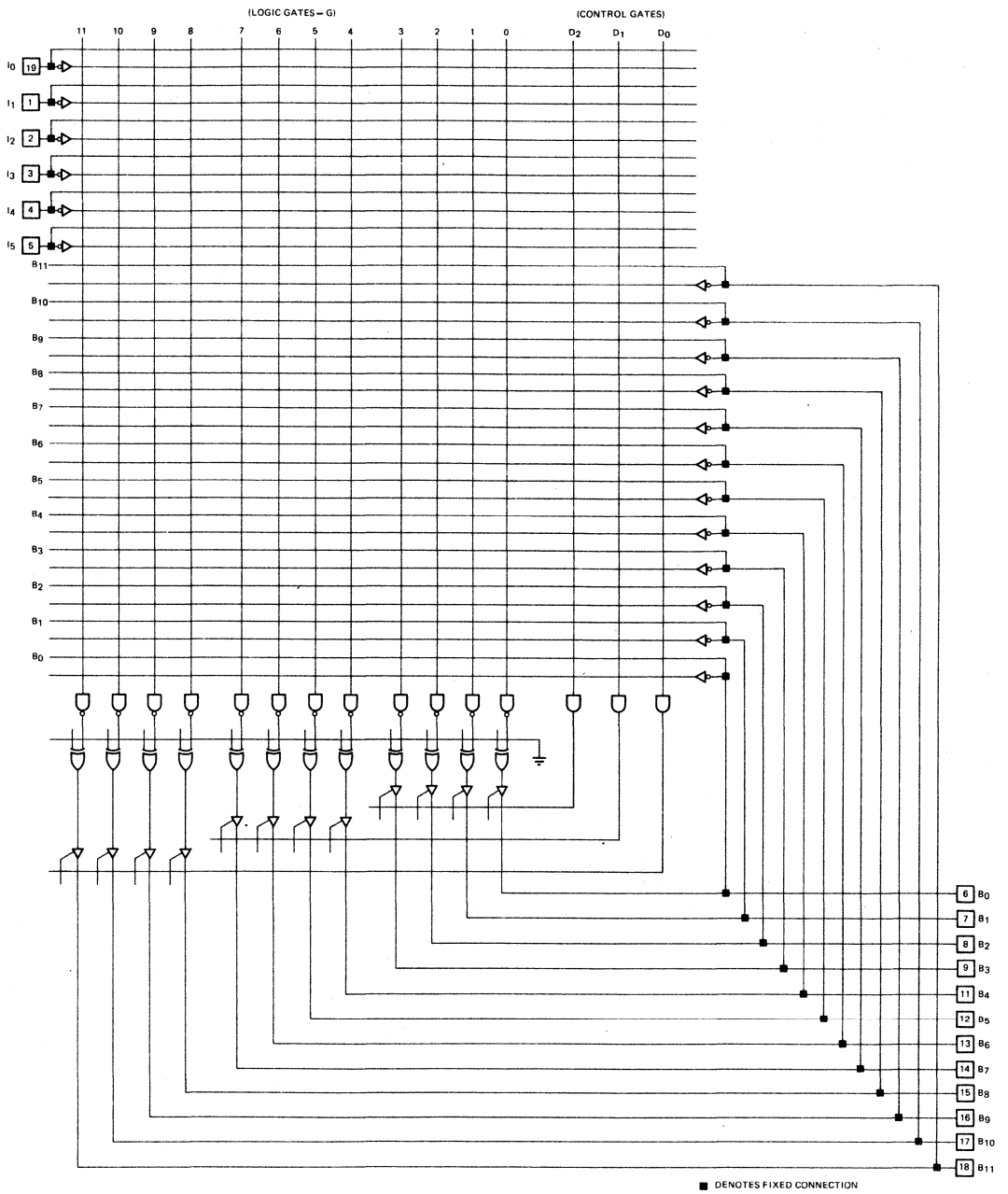
NOTES:
1. For each of the 12 outputs, either function X (active-high) or $\overline{X}$ (active-low) is available, but not both. The desired output polarity is programmed via link (L).
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



NOTES:
1. ■ Denotes fixed connection
2. All Ni-Cr links are initially intact.

PGA LOGIC DIAGRAM



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGI(
SERIES 20

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			C°
T_A	Operating			
	N82S150/151	0	+75	
	S82S150/151	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	Military	Commercial
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHACTERISTICS

N82S150/151: 0°C− Ta ≤ +75°C, 4.75 ≤ V_{CC} ≤ 5.25V
S82S150/151: −55°C ≤ Ta ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITION	N82S150/151 Min	N82S150/151 Typ[2]	N82S150/151 Max	S82150/151 Min	S82150/151 Typ[2]	S82150/151 Max	UNIT
	Input voltage[3]								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[3,4]	V_{CC} = Min, Iin = −18mA		.8	−1.2		.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[3,5]	I_{OL} = 10mA			.5				
V_{OL}	Low[3,5]	I_{OL} = 10mA						.5	
V_{OH}	High[3,6]	I_{OH} = −2mA	2.4			2.4			
	Input Current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output Current	V_{CC} = max							
I_{OLK}	Leakage (82S150)	V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S151)	V_{OUT} = 5.5V			40			60	μA
		V_{OUT} = .45V			−40			−60	
I_{OS}	Short circuit (82S151)[4,6,7]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = max		130	155		130	155	mA
	Capacitance	V_{CC} = 5V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_B	I/O	V_B = 2.0V		15			15		

AC ELECTRICAL CHACTERISTICS

R_1 = 470Ω, R_2 = 1KΩ
N82S150/151: 0°C ≤ Ta ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S150/151: −55°C ≤ Ta ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	TEST CONDITIONS	N82S150/151 Min	N82S150/151 Typ[2]	N82S150/151 Max	S82S150/151 Min	S82S150/151 Typ[2]	S82S150/151 Max	UNIT
T_{PD}	Progagation delay	Output±	Input±	C_L = 30pF		25	30		25		ns
T_{OE}	Output enable	Output−	Input±			20	25		25		ns
T_{OD}	Output disable[9]	Output+	Input±	C_L = 5pF		20	25		25		

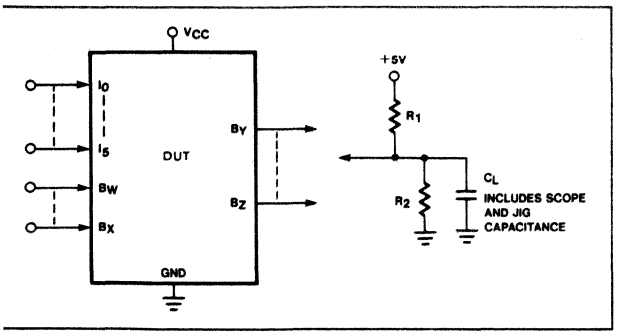
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 26°C
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5.
6.
7. Duration of short circuit should not exceed 1 second.
8.
9. Measured at V_T = V_{OL} + 0.5V.

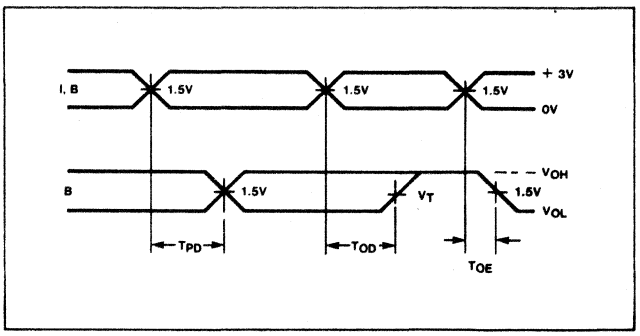
OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

TEST LOAD CIRCUIT



TIMING DIAGRAM



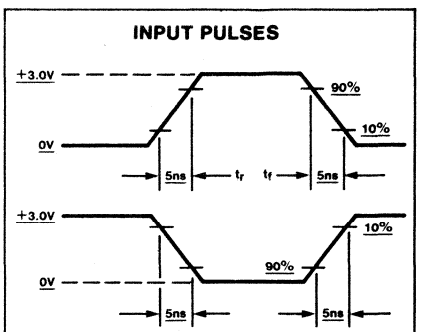
TIMING DEFINITIONS

TPD Propagation delay between input and output.

TOD Delay between input change and when output is off (Hi-Z or High).

TOE Delay between input change and when output reflects specified output level.

VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

LOGIC PROGRAMMING

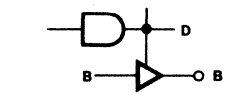
In a virgin device all Ni-Cr links are intact.

The FPLA can be programmed by means of Logic programming equipment.

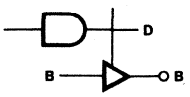
With Logic programming, the AND/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this Table the logic state or action of variables I and B associated with each gate Gn, Dn is assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:

I/O DIRECTION—(B)

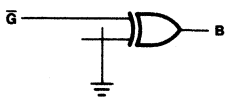


DIRECTION	CODE
I/O	A

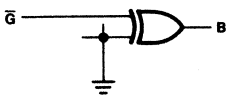


DIRECTION	CODE
OUTPUT	●

EX-OR ARRAY—(B)

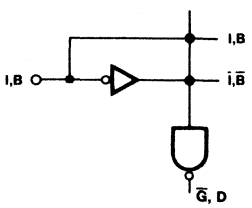


ACTIVE LEVEL	CODE
HIGH	H

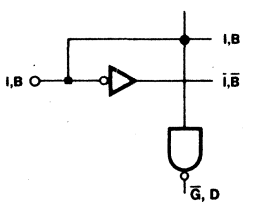


ACTIVE LEVEL	CODE
LOW	L

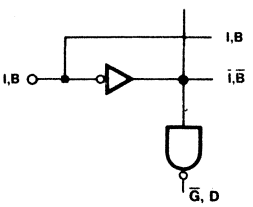
"AND" ARRAY—(I,B)



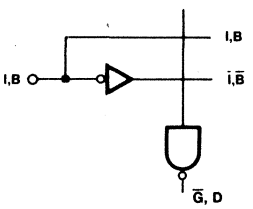
STATE	CODE
INACTIVE	O



STATE	CODE
I,B	H



STATE	CODE
$\bar{I},\bar{B}$	L



STATE	CODE
DON'T CARE	—

NOTES

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates Gn, Dn.
2. Any gate Gn, Dn will be unconditionally inhibited if any one of its (I, B) link pairs is left intact.

BJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

PGA PROGRAM TABLE (Logic)

PROGRAM TABLE ENTRIES:

I, B (AND)	
INACTIVE	0
I, B	H
$\bar{I}, \bar{B}$	L
Don't Care	–

G (or B) (POL.)	
HIGH	H
LOW	L

G (or B) (DIR.)	
I/O	A
OUTPUT	●

NOTES:
1. The FPGA is shipped with all links initially intact. Thus a background of "O" for all Gates, an "A" for Direction, and "L" for Output Polarity exists in the table, shown BLANK for clarity.
2. Unused I_m and B_n bits are normally programmed Don't Care (—).
3. Unused Gates can be left blank.
4. Disregard Polarity for Gates used only as inputs.

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

D2 = _____

G0 = _____

G1 = _____

G2 = _____

G3 = _____

D1 = _____

G4 = _____

G5 = _____

G6 = _____

G7 = _____

D0 = _____

G8 = _____

G9 = _____

G10 = _____

G11 = _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE ____

PIN	GATE	DIR.	POL.	AND I 5	I 4	I 3	I 2	I 1	I 0	B 11	B 10	B 9	B 8	B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0
	D2																				
6	00																				
7	01																				
8	02																				
9	03																				
	D1																				
11	04																				
12	05																				
13	06																				
14	07																				
	D0																				
15	08																				
16	09																				
17	10																				
18	11																				
		PIN		5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	8	7	6

BIPOLAR MEMORY

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S152 and 82S153 are two-level logic elements, consisting of 32 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for inplementing AND-OR or AND-NOR logic functions.

The 82S152 and the 82S153 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Both devices are available in a 20 pin slim line package. For the commercial temperature range (0°C to +75°C) specify N82S152/153 N or F. For the military temperature range (−55°C to +125°C) specify S82S152/153 F only.

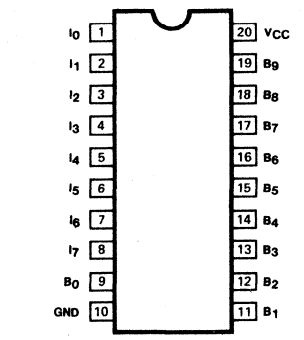
FEATURES

- **Field programmable (Ni-Cr links)**
- **8 inputs**
- **32 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active high or low outputs**
- **I/O propagation delay:**
  N82S152/153: 40ns (max)
  S82S152/153: ns (max)
- **Input loading**
  N82S152/153: −100A (max)
  S82S152/153: −150A (max)
- **Power dissipation:**
  650mW (typ)
- **Output options:**
  82S152: open collector
  82S153: tri-state
- **TTL compatible**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

PIN CONFIGURATION



F = Cerdip
N = Plastic

LOGIC FUNCTION

Typical product term:

$Pn = A \bullet \overline{B} \bullet C \bullet D \bullet \ldots$

Typical logic function:

At L = Closed

$X = P0 + P1 + P2 \ldots$

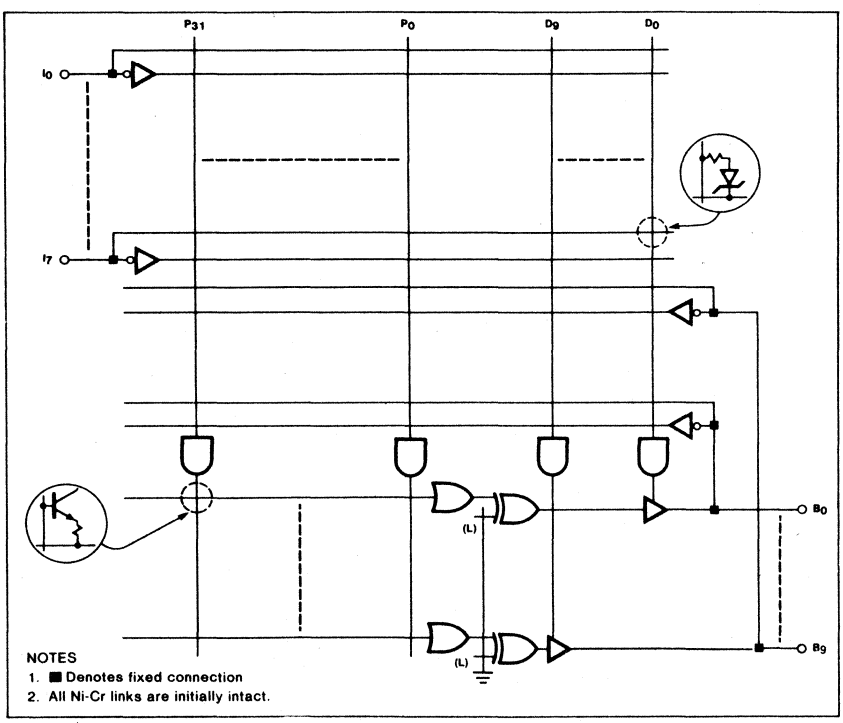
At L = Open

$X = \overline{P0 + P1 + P2 + \ldots}$

$X = \overline{P0} \bullet \overline{P1} \bullet \overline{P2} \ldots$

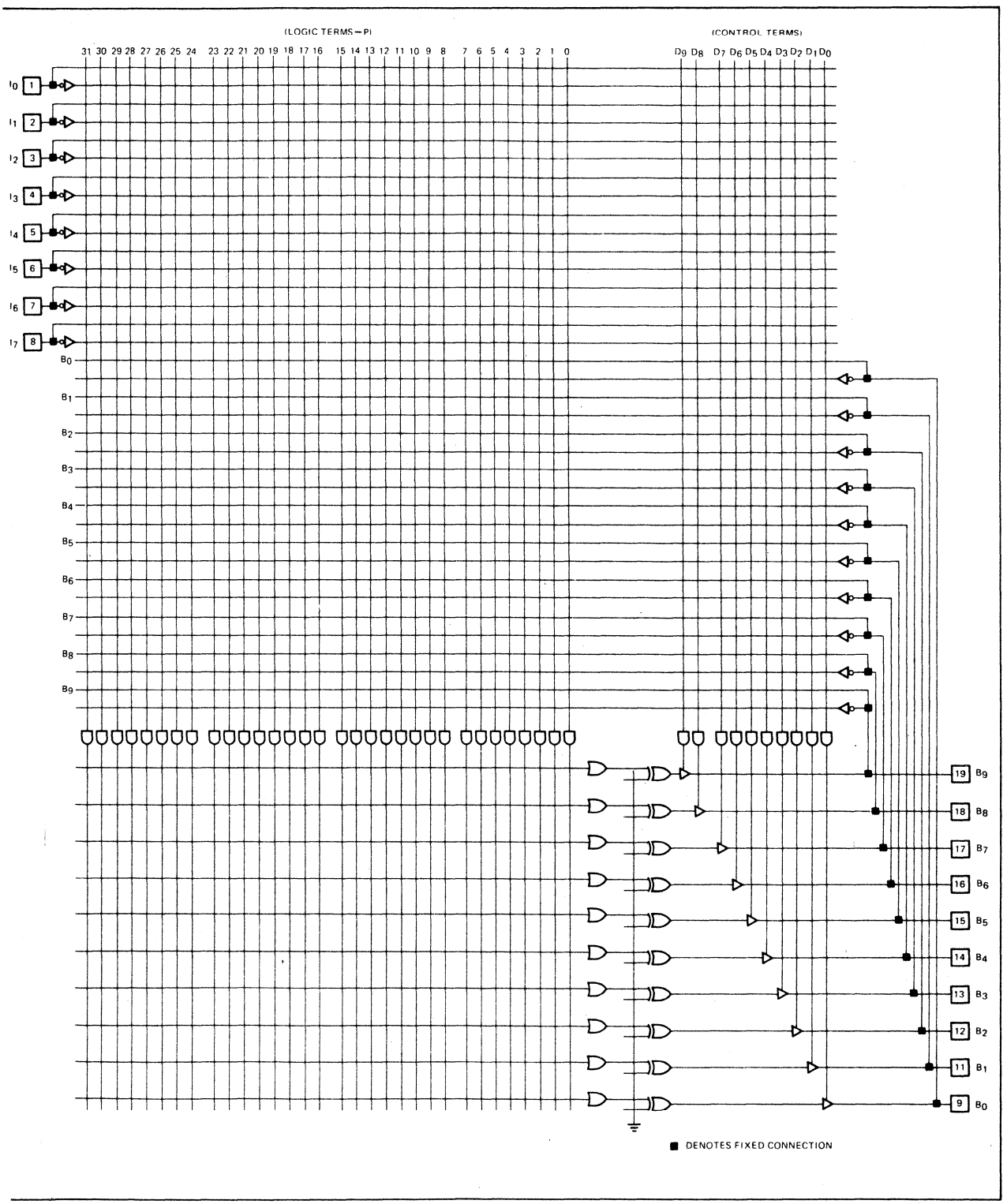
NOTES
1. For each of the 10 outputs, either function X (active high) or $\overline{X}$ (active low) is available, but not both. The desired output polarity is programmed via link (L).
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



NOTES
1. ■ Denotes fixed connection
2. All Ni-Cr links are initially intact.

FPLA LOGIC DIAGRAM



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			C°
T_A	Operating			
	N82S152/153	0	+75	
	S82S152/153	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	Military	Commercial
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S152/153: $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$
S82S152/153: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITION	N82S152/153 Min	N82S152/153 Typ[2]	N82S152/153 Max	S82S152/153 Min	S82S152/153 Typ[2]	S82S152/153 Max	UNIT
	Input voltage[3]								V
V_{IL}	Low	V_{CC} = min			.85			.80	
V_{IH}	High	V_{CC} = max	2.0			2.0			
V_{IC}	Clamp[3,4]	V_{CC} = min, Iin = −18mA		.8	−1.2		.8	−1.2	
	Output voltage	V_{CC} = min							V
V_{OL}	Low[3,5]	I_{OL} = 10mA			.5				
V_{OL}	Low[3,5]	I_{OL} = 10mA						.5	
V_{OH}	High[3,6]	I_{OH} = −2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current	V_{CC} = max							
I_{OLK}	Leakage (82S152)	V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S153)	V_{OUT} = 5.5V			40			60	μA
		V_{OUT} = .45V			−40			−60	
I_{OS}	Short circuit (82S153)[4,6,7]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = max		130	155		130	155	mA
	Capacitance	V_{CC} = 5V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_B	I/O	V_B = 2.0V		15			15		

AC ELECTRICAL CHACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1K\Omega$
N82S152/153: $0° C \leq Ta \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S152/153: $-55°C \leq Ta \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	TEST CONDITIONS	N82S150/151 Min	N82S150/151 Typ	N82S150/151 Max	S82S150/151 Min	S82S150/151 Typ	S82S150/151 Max	UNIT
T_{PD}	Progagation delay	Output±	Input±	C_L = 30pF		25	30		25		ns
T_{OE}	Output enable	Output−	Input±			20	25		25		ns
T_{OD}	Output disable[9]	Output+	Input±	C_L = 5pF		20	25		25		

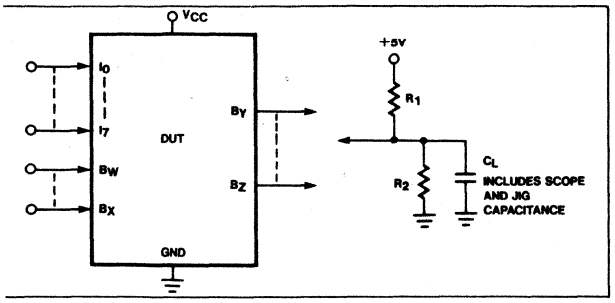
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with +10V applied to I_7.
6. Measured with +10V applied to I_{0-7}. Output sink current is supplied thru a resistor to V_{CC}.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with I_{0-7} and B_{0-9} at 4.5V.
9. Measured at $V_T = V_{OL} + 0.5V$.

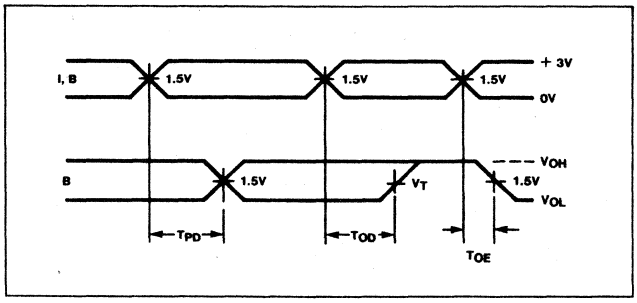
OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

TEST LOAD CIRCUIT



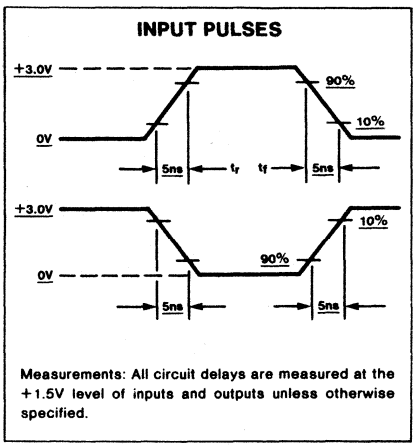
TIMING DIAGRAM



TIMING DEFINITIONS

tPD	Propagation delay between input and output.
tOD	Delay between input change and when output is off (Hi-Z or High).
tOE	Delay between input change and when output reflects specified output level.

VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs unless otherwise specified.

BIPOLAR MEMORY

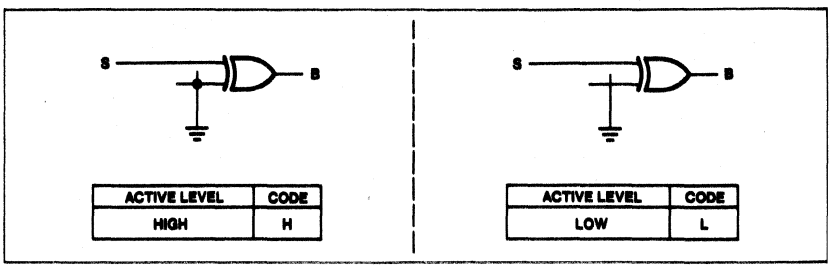
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this Table the logic state or action of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

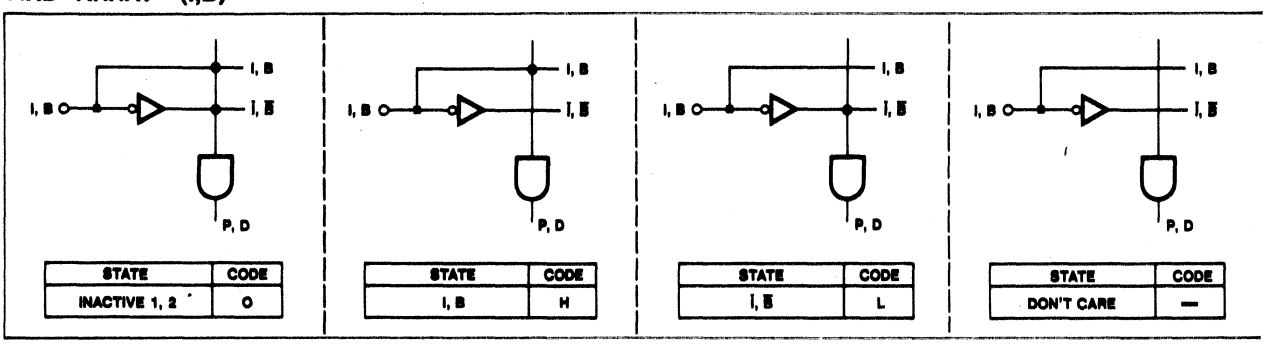
EX-OR ARRAY - (B)



ACTIVE LEVEL	CODE
HIGH	H

ACTIVE LEVEL	CODE
LOW	L

"AND" ARRAY - (I,B)



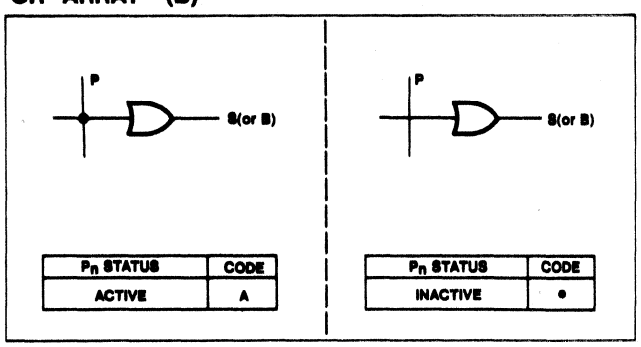
STATE	CODE
INACTIVE 1, 2	O

STATE	CODE
I, B	H

STATE	CODE
$\bar{I}$, $\bar{B}$	L

STATE	CODE
DON'T CARE	—

"OR" ARRAY - (B)



P_n STATUS	CODE
ACTIVE	A

P_n STATUS	CODE
INACTIVE	•

NOTES

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if any one of its (I, B) link pairs is left intact.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

FPLA PROGRAM TABLE (Logic)

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ___ DATE ___

PROGRAM TABLE ENTRIES:

I, B(I) (AND)		B(O) (OR)		B(O) (POL.)	
INACTIVE	0	ACTIVE	A	HIGH	H
I_m, B_n	H	INACTIVE	B	LOW	L
$\bar{I}_m$, $\bar{B}_n$	L				
Don't Care	–				

NOTES
1. The FPLA is shipped with all links initially intact. Thus a background of "O" for all Terms, and "H" for output polarity exists in the table, shown BLANK for clarity.
2. Unused I_m and B_n bits in the AND array are normally programmed Don't Care (-).
3. Unused product terms can be left blank.

TERM	AND I 7	6	5	4	3	2	1	0	AND B(I) 9	8	7	6	5	4	3	2	1	0	POLARITY	OR B(O) 9	8	7	6	5	4	3	2	1	0
0																													
1																													
2																													
3																													
4																													
5																													
6																													
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D5																													
D4																													
D3																													
D2																													
D1																													
D0																													
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9											

DESCRIPTION

The 82S154/155/156/157/158/159 are Open Collector and Tri-state registered logic elements combining AND/OR gate arrays with clocked J/K flip-flops, optionally convertible to D-type via a "foldback" inverting buffer. They all have similar organization, featuring respectively 4, 6, or 8 registered I/O outputs (F), in conjunction with 8, 6, or 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 AND gates and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of OR gates drives bidirectional I/O lines (B), whose output polarity is individually programmable thru a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R), (except the 82S158/159, where AND functions are provided).

All flip-flops are positive edge trigger and can be used as input, output, or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering input (I) and programmable output select lines (E).

The 82SXXX are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

All devices are available in a 20-pin, slim line package. For the commercial temperature range (0°C to +75°C) specify N82SXXX N or F. For the military temperature range (−55°C to +125°C) specify S82SXXX F only.

FLIP-FLOP TRUTH TABLE

V_{CC}	$\overline{O.E.}$	L	CK	P	R	J	K	Q	F
	H								H/HI-Z
↑	L	X	X	X	L	X	X	H	L
+5	L	X	X	H	L	X	X	H	L
	L	X	X	L	H	X	X	L	H
	L	L	↑	L	L	L	L	Q	$\overline{Q}$
	L	L	↑	L	L	L	H	L	H
	L	L	↑	L	L	H	L	H	L
	L	L	↑	L	L	H	H	$\overline{Q}$	Q
	H	H	↑	L	L	L	H	L	H*
	H	H	↑	L	L	H	L	H	L*

NOTES
1. Positive Logic:
   $J/K = T_0 + T_1 + T_2 \ldots\ldots\ldots T_{47}$
   $T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (Q_0 \bullet Q_1 \ldots) \bullet (B_0 \bullet B_1 \bullet \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't Care
4. * = Forced at I/O pin to load J/K flip-flop when L is enabled via steering input(s) I,B.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.

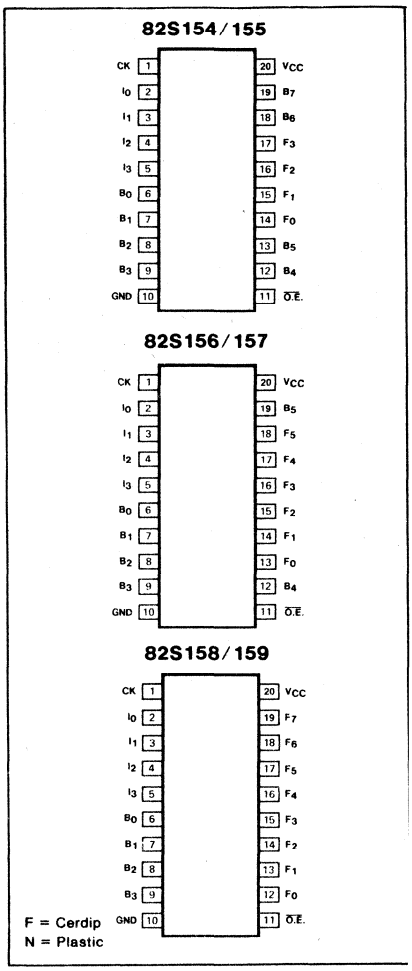
FEATURES

- Field programmable (Ni-Cr link)
- 4 Inputs
- 32 AND gates
- 21 OR gates
- Bidirectional I/O lines:
  - 82S154/155—8
  - 82S156/157—6
  - 82S158/159—4
- Bidirectional Registers:
  - 82S154/155—4
  - 82S156/157—6
  - 82S158/159—8
- J/K, T, or D-type flip-flops
- Asynchronous Preset/Reset
- Complement Array
- Active high or low outputs
- Programmable $\overline{O.E.}$ control
- Positive edge trigger clock
- Power-on preset to all "1"
- Clock frequency:
  - N82SXXX: 15 MHz (max)
  - S82SXXX: MHz (max)
- Input loading:
  - N82SXXX: −100μA (max)
  - S82SXXX: −150μA (max)
- Power dissipation: 650mW (typ)
- Output options:
  - 82S154/6/8: Open Collector
  - 82S155/7/9: Tri-state
- TTL Compatible

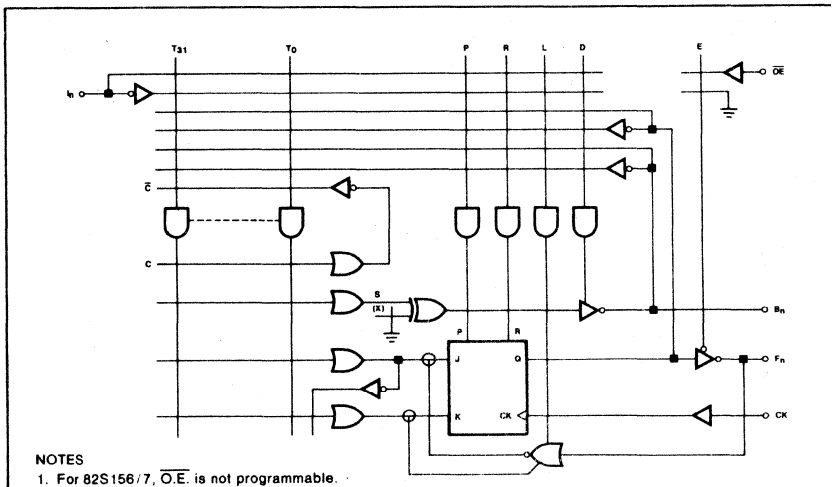
APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



NOTES
1. For 82S156/7, $\overline{O.E.}$ is not programmable.
2. For 82S154/5/6/7, P and R are "OR" functions.

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**CLOCK** The clock input to all flip-flops. A Low-to-High transition on this line is necessary to update the contents of flip-flops.	Active-High
2-5	I_{0-3}	**INPUTS** Fixed logic inputs to the AND array	Active-High/Low (user defined)
6-9	B_{0-3}	**STATIC I/O PINS** Bidirectional external inputs to the AND array, or outputs from the OR array, programmable via control gates D_{0-3}.	Active-High/Low (user defined)
11	$\overline{O.E.}$	**$\overline{\text{OUTPUT ENABLE}}$** Provides output enable functions E_A and E_B to flip-flop banks F_{0-3} and F_{4-7} respectively. May be programmed for external control, enable, or disable of flip-flop outputs.	Active-Low
12, 13	$(B_n/F_n)^*$	**STATIC OR REGISTERED I/O PINS** Bidirectional static or registered I/O pins, dependent on device configuration.	Active-High/Low (user defined)
14-17	$(F_n)^*$	**REGISTERED I/O PINS** Bidirectional flip-flop outputs or direct load inputs, selected via control gates L_{A-B} in conjunction with E_{A-B} output enables.	Active-Low
18, 19	$(B_n/F_n)^*$	**STATIC OR REGISTERED I/O PINS** Same as 12, 13.	Active-High/Low (user defined)

(*) Value of (n) is device dependent. Refer to circuit diagrams.

LOGIC FUNCTION

COMBINATORIAL

Typical Product Term: $P_n = A \bullet \overline{B} \bullet \overline{C} \bullet D \bullet \overline{E} \bullet \ldots.$

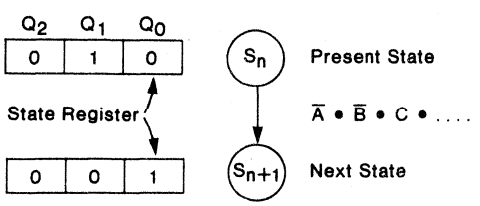
Typical Logic Function: At X = Open $Y = P_0 + P_1 + P_2 + \ldots.$

at D_Y = "1" At X = Closed $Y = \overline{P_0 + P_1 + P_2 + \ldots.}$

$= \overline{P}_0 \bullet \overline{P}_1 \bullet \overline{P}_2 \bullet \ldots.$

SEQUENTIAL (J/K type)

Typical State Transition:



$\overline{A} \bullet \overline{B} \bullet C \bullet \ldots.$

SET Q_0: $J_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$
$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

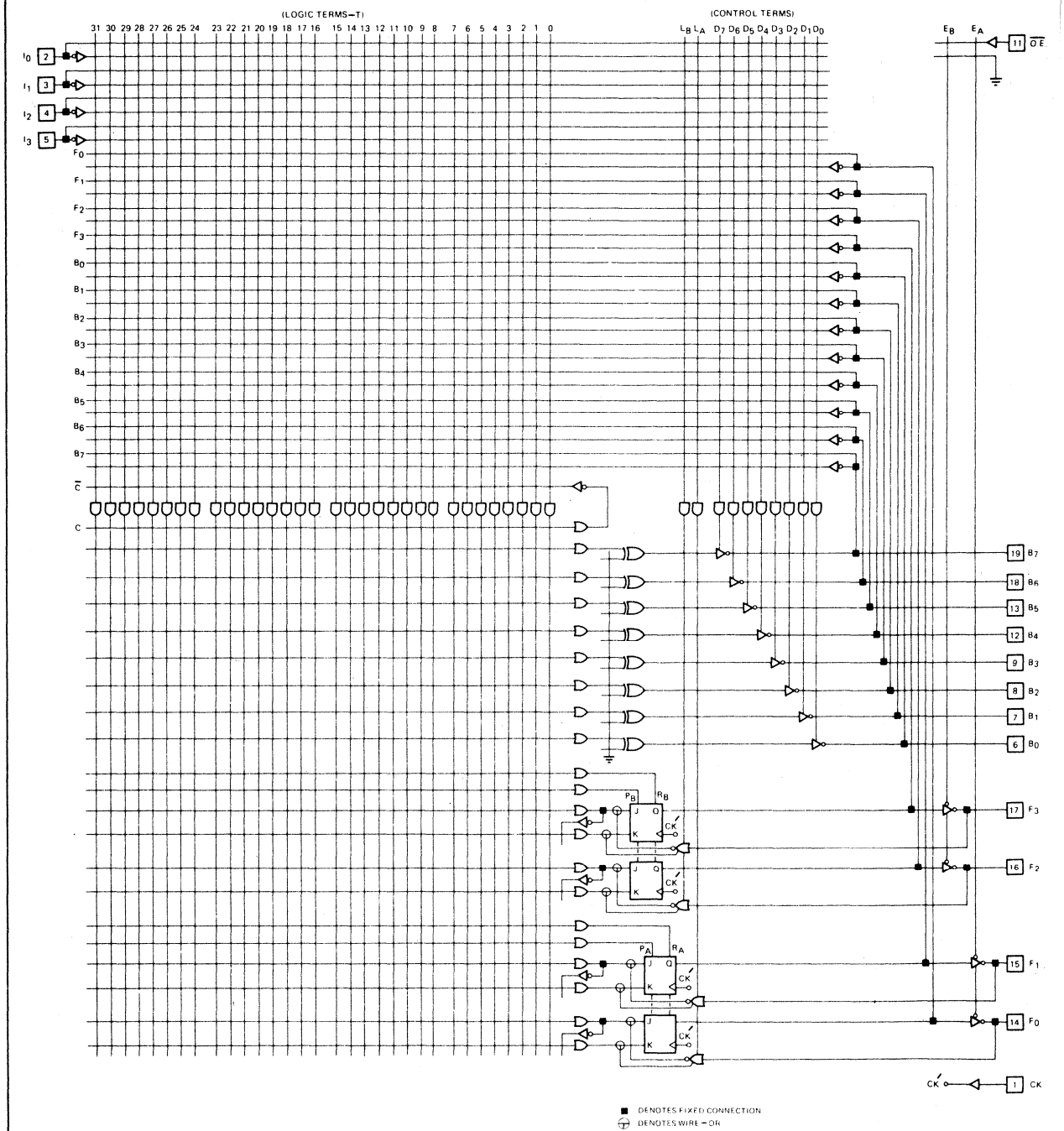
NOTES
1. For each of the combinatorial outputs, either function L (active-high) or $\overline{L}$ (active-low) is available, but not both. The desired output polarity is programmed via link (X).
2. L, A, B, C, etc. are user defined connections to fixed inputs (I), bidirectional pins (B), "foldback" register outputs (Q), and Complement Array ($\overline{C}$).
3. Sequential state transitions occur on the positive edge of clock. External flip-flop outputs are given by $F_n = \overline{Q}_n$.
4. For D-type flip-flops, $K_n = \overline{J}_n$. For T-type flip-flops, $K_n = J_n$.

OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

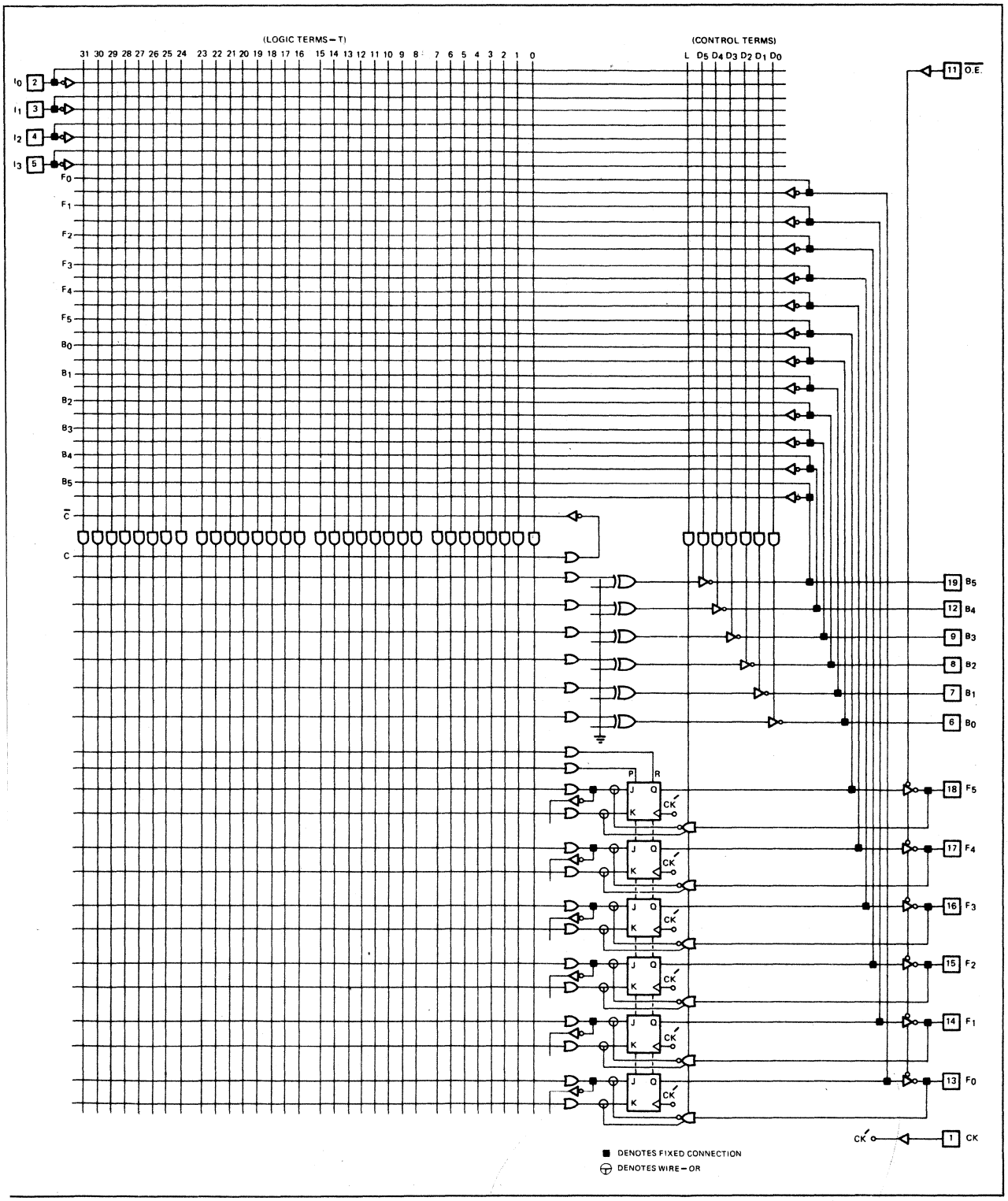
FPLS LOGIC DIAGRAM

82S154/155



FPLS LOGIC DIAGRAM

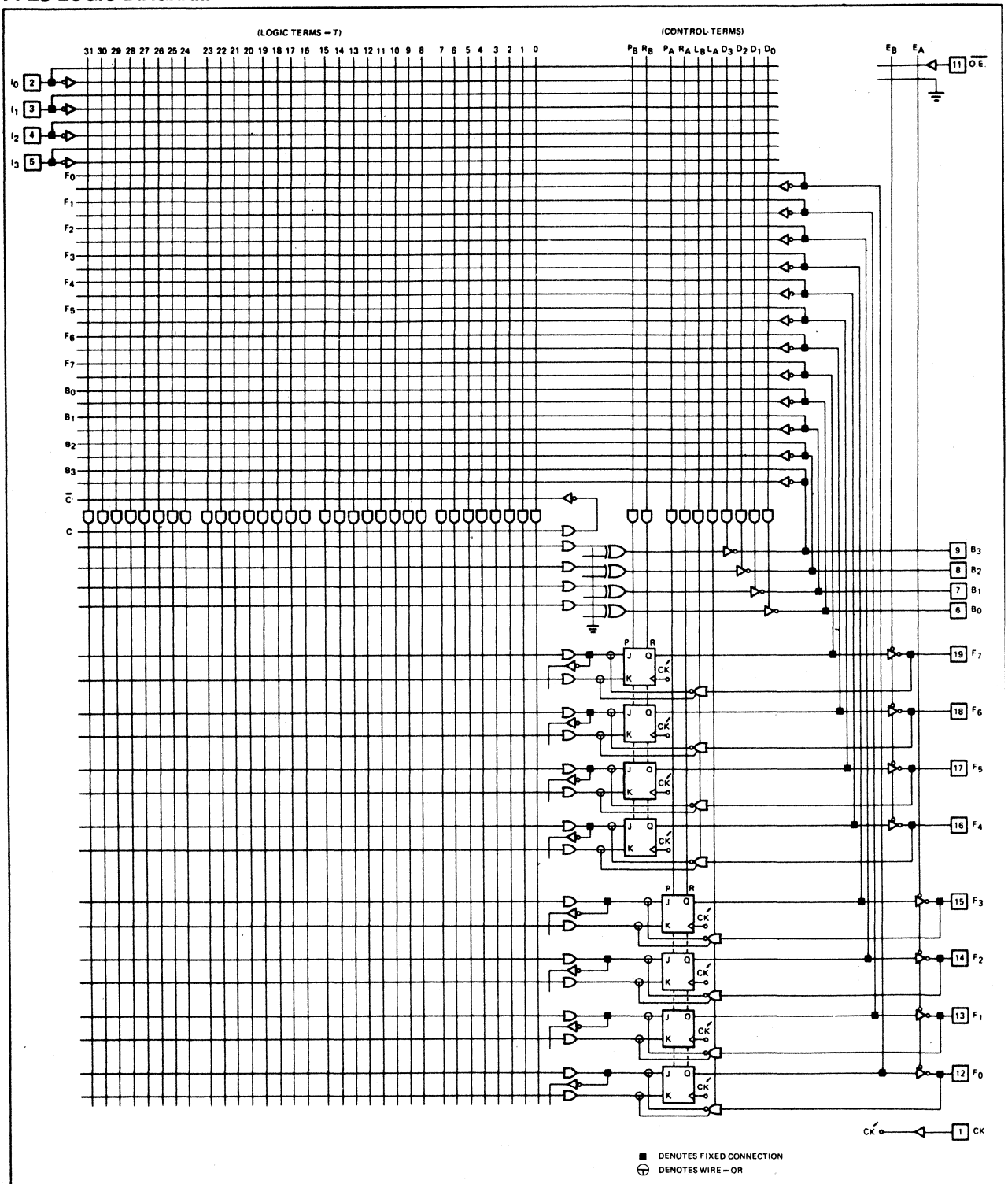
82S156/157



BIPOLAR MEMORY

FPLS LOGIC DIAGRAM

82S158/159



OBJECTIVE SPECIFICATION

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S154/5/6/7/8/9	0	+75	
	S82S154/5/6/7/8/9	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S154/5/6/7/8/9: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S154/5/6/7/8/9: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S154/5/6/7/8/9 Min	N82S154/5/6/7/8/9 Typ[2]	N82S154/5/6/7/8/9 Max	S82S154/5/6/7/8/9 Min	S82S154/5/6/7/8/9 Typ[2]	S82S154/5/6/7/8/9 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S155/7/9)[3,5]	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 10mA		0.35	0.5				
V_{OL}	Low[3,6]	I_{OL} = 10mA					0.35	0.5	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	40		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250		−50	−350	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S155/7/9)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S155/7/9)[4,6,7]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		130	155		130	155	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		15			15		

NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5.
6.
7. Measured with V_{IH} applied to $\overline{O.E.}$
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the $\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.

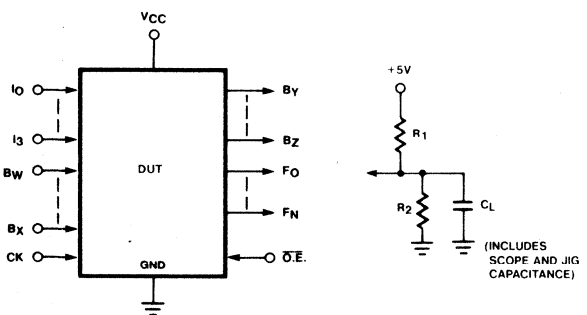
AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$
N82S154/5/6/7/8/9: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S154/5/6/7/8/9: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

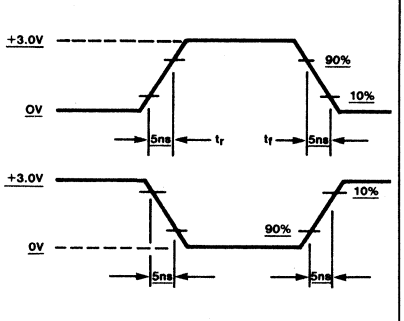
	PARAMETER	TO	FROM	TEST CONDITIONS	N82S154/5/6/7/8/9/ Min	N82S154/5/6/7/8/9/ Typ[1]	N82S154/5/6/7/8/9/ Max	S82S154/5/6/7/8/9 Min	S82S154/5/6/7/8/9 Typ[1]	S82S154/5/6/7/8/9 Max	UNIT
	Pulse width										ns
T_{CKH}	Clock[2] high	CK−	CK+		25	20			20		
T_{CKL}	Clock low	CK+	CK−		25	20			20		
T_{CKP}	Period	CK+	CK+		65	50			50		
T_{PRH}	Preset/Reset pulse	(I,B)+	(I,B)−		25	20			20		
	Set up time										ns
T_{IS1}	Input	CK+	(I,B)±	C_L = 30pF	35	30			30		
T_{IS2}	Input (through F_n)	CK+	F±	C_L = 30pF	10	5			5		
	Hold time										ns
T_{IH1}	Input	CK+	(I,B)±	C_L = 30pF		−10	0		−10		
T_{IH2}		CK+	F±	C_L = 30pF		−5	0		−5		
	Propagation delay										ns
T_{CKO}	Clock	F±	CK+	C_L = 30pF		25	30		25		
T_{OE1}	Output enable	F−	$\overline{O.E.}$−	C_L = 30pF		20	25		20		
T_{OD1}	Output disable[3]	F+	$\overline{O.E.}$+	C_L = 5pF		20	25		20		
T_{PD}	Output	B±	(I,B)±	C_L = 30pF		35	40		35		
T_{OE2}	Output enable	B±	(I,B)+	C_L = 30pF		35	40		35		
T_{OD2}	Output disable[3]	B+	(I,B)−	C_L = 5pF		35	40		35		
T_{PRO}	Preset/Reset	F±	(I,B)+	C_L = 30pF		50	65		50		
T_{PPR}	Power-on preset	F−	V_{CC}+	C_L = 30pF		0	10		0		

NOTE
1. All typical values are at V_{CC} = 5V, T_A = 25°C.
2. To prevent spurious clocking, clock rise time (10%-90%) ≤ 10ns.
3. Measured at $V_T = V_{OL} + 0.5V$.

TEST LOAD CIRCUIT

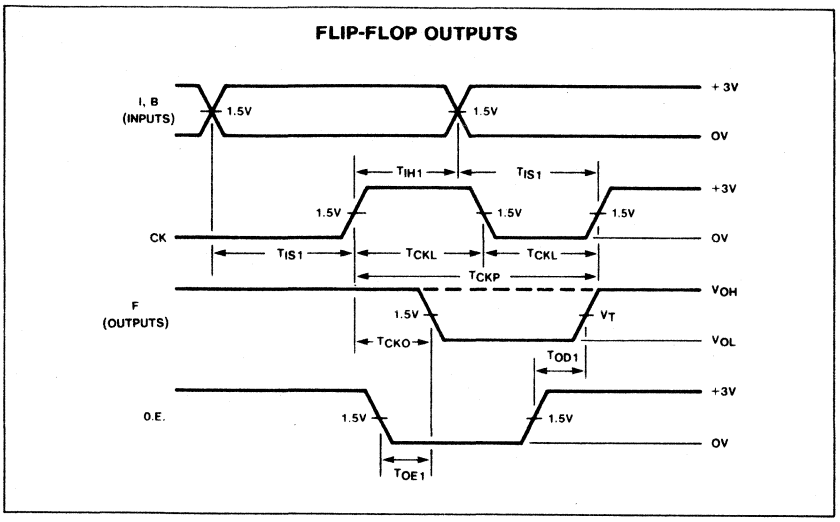


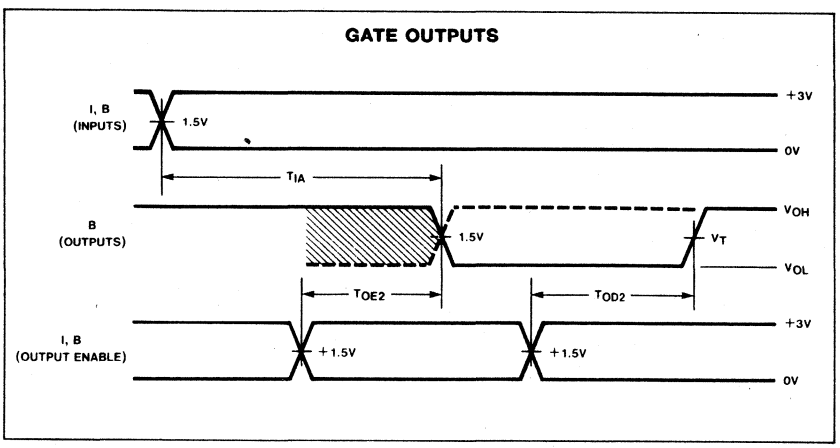
VOLTAGE WAVEFORM

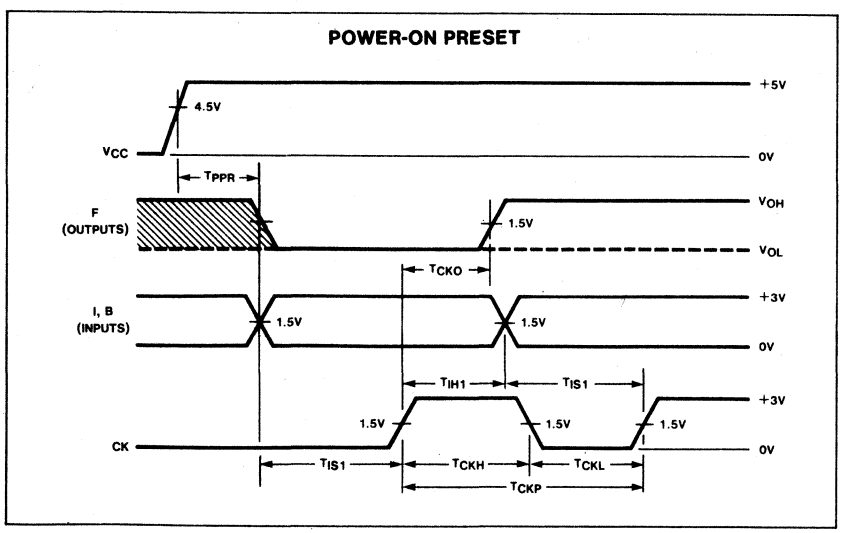


Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

TIMING DIAGRAMS







MEMORY TIMING DEFINITIONS

T_{CKH} Width of input clock pulse.
T_{CKL} Interval between clock pulses.
T_{CKP} Clock period.

T_{PRH} Width of preset input pulse.

T_{IS1} Required delay between beginning of valid input and positive transition of clock.

T_{IS2} Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.

T_{IH1} Required delay between positive transition of clock and end of valid input data.

T_{IH2} Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.

T_{CKO} Delay between positive transition of clock and when Outputs become valid (with $\overline{O.E.}$ low).

T_{OE1} Delay between beginning of Output Enable Low and when Outputs become valid.

T_{OD1} Delay between beginning of Output Enable High and when Outputs are in the off state.

T_{PD} Propagation delay between combinational inputs and outputs.

T_{OE2} Delay between predefined Output Enable High, and when combinational Outputs become valid.

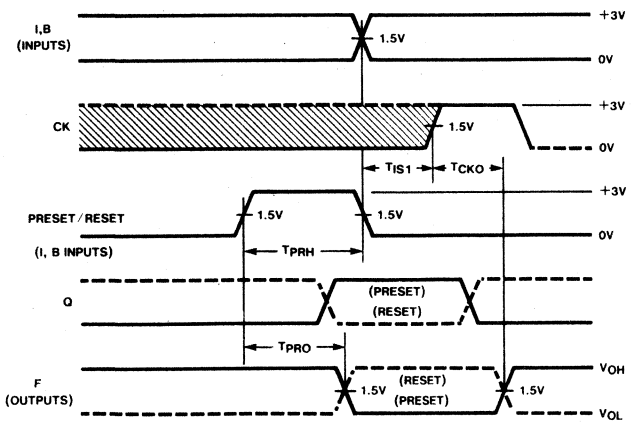
T_{OD2} Delay between predefined Output Enable Low and when combinational Outputs are in the off state.

T_{PRO} Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

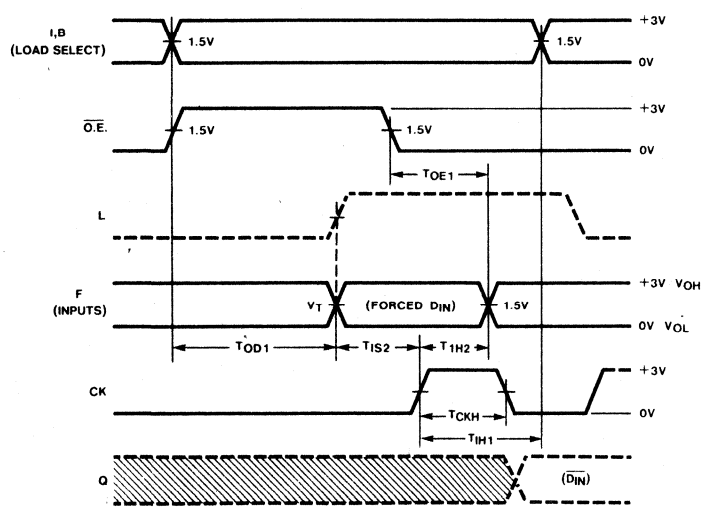
T_{PPR} Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "0" (internal Q outputs at "1").

TIMING DIAGRAMS (Cont'd)

ASYNCHRONOUS PRESET/RESET



FLIP-FLOP INPUT MODE



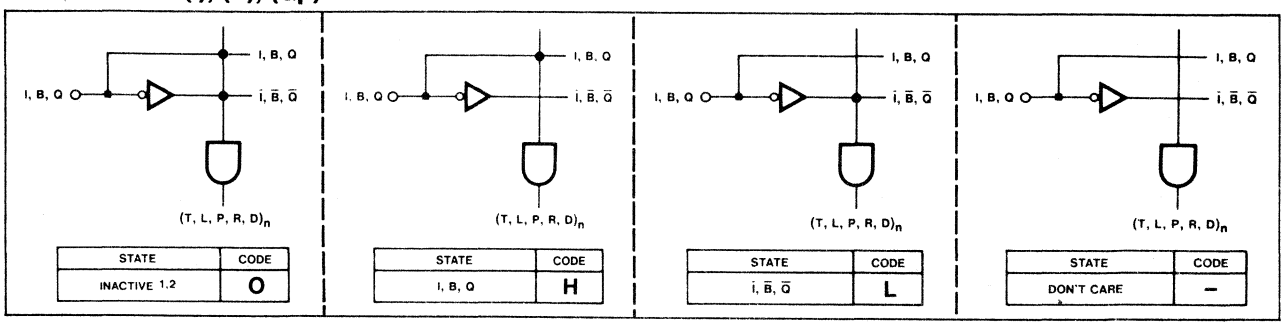
LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic Programming equipment.

With Logic programming, the AND/OR/EX-OR input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Tables on the following pages.

In this Table, the logic state or action of all I/O, control, and state variables is assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:

"AND" ARRAY - (I), (B), (Qp)



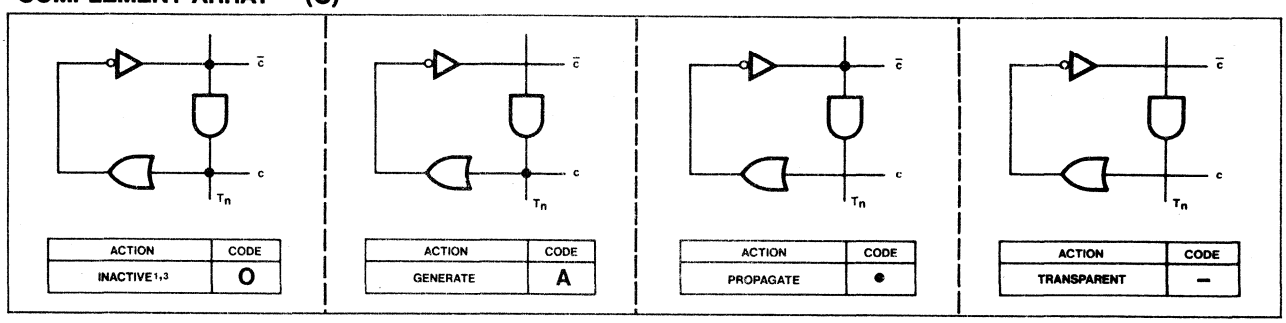
STATE	CODE
INACTIVE 1,2	O

STATE	CODE
I, B, Q	H

STATE	CODE
i, B̄, Q̄	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT ARRAY" - (C)



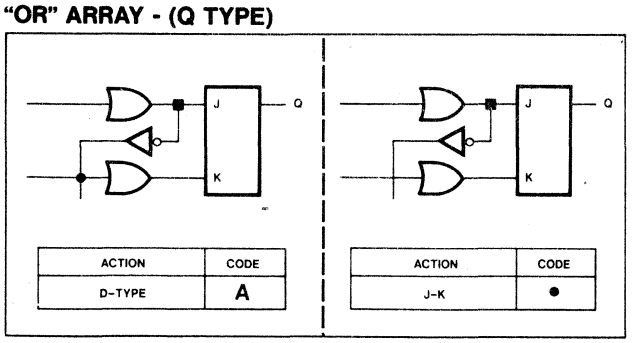
ACTION	CODE
INACTIVE1,3	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

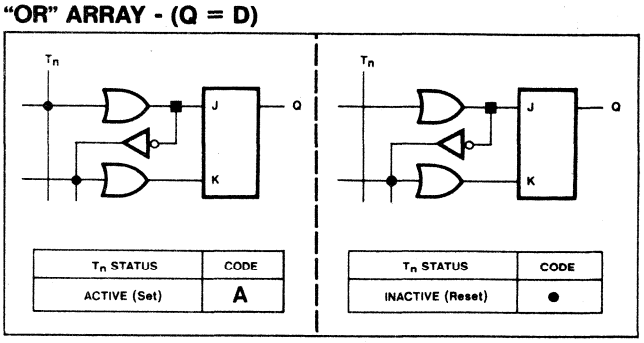
"OR" ARRAY - (Q TYPE)



ACTION	CODE
D-TYPE	A

ACTION	CODE
J-K	•

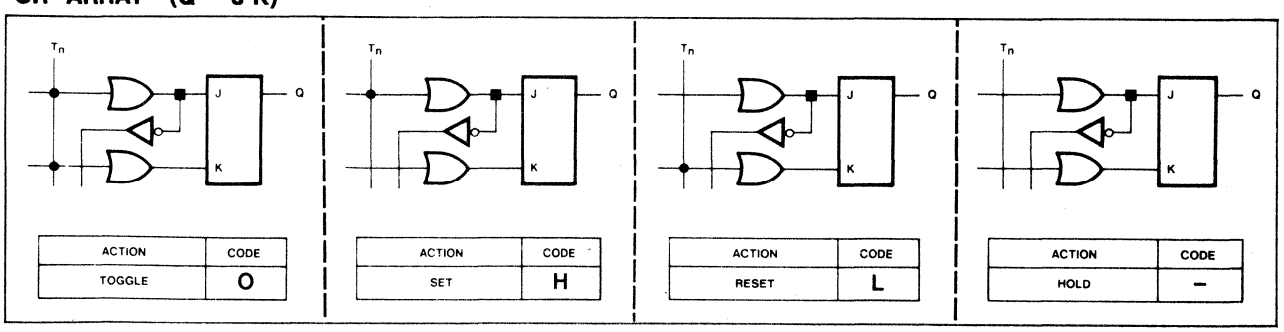
"OR" ARRAY - (Q = D)



Tn STATUS	CODE
ACTIVE (Set)	A

Tn STATUS	CODE
INACTIVE (Reset)	•

"OR" ARRAY - (Q = J-K)



ACTION	CODE
TOGGLE	O

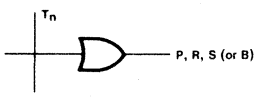
ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

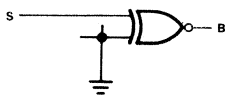
"OR" ARRAY - (S or B), (P), (R)

T_n STATUS	CODE
ACTIVE	A

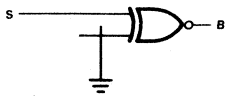


T_n STATUS	CODE
INACTIVE	•

"EX-OR" ARRAY - (B)

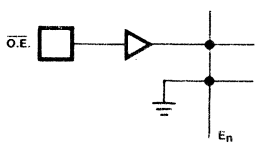


POLARITY	CODE
LOW	L

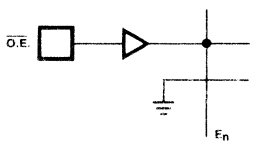


POLARITY	CODE
HIGH	H

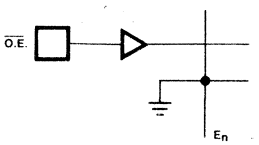
"$\overline{O.E.}$" ARRAY - (E)



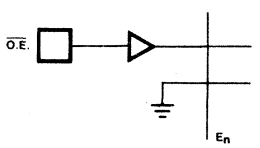
ACTION	CODE
IDLE[4]	O



ACTION	CODE
CONTROL	A



ACTION	CODE
ENABLE[4]	•



ACTION	CODE
DISABLE	–

NOTES

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
2. Any gate $(T, L, P, R, D)_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. Links in the $\overline{O.E.}$ array are not isolated from each other, so that $E_A = 0$ and $E_A = \bullet$ are logically equivalent. Thus if register bank A is enabled with $E_A = 0$, then E_B can either be idle, enabled or disabled, but not controlled (and vice versa).

FPLS PROGRAM TABLE (Logic)

82S154/155

PROGRAM TABLE ENTRIES:

I, Q, B(I) (AND)

INACTIVE	O
I, F, B	H
$\bar{I}$, $\bar{F}$, $\bar{B}$	L
DON'T CARE	–

C (AND)

INACTIVE	O
GENERATE	A
PROPAGATE	●
TRANSPARENT	–

(O = J/K) (AND)

TOGGLE	O
SET	H
RESET	L
HOLD	–

$\overline{O.E.}$

IDLE	O
CONTROL	A
ENABLE	●
DISABLE	–

P, R, B(O), (Q = D) (OR)

ACTIVE	A
INACTIVE	●

B(O) (POL.)

HIGH	H
LOW	L

F/F TYPE (OR)

J/K	●
D	A

NOTES
1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (–). Program unused Q, B, P, and R bits in the OR array as (–) or (A), as applicable.
3. Unused Terms can be left blank.
4. If E_A = (0), E_B cannot be controlled, and vice versa.
5. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

($\overline{O.E.}$) (F/F TYPE) | E_B = | E_A = | (POLARITY)

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____ CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE ____

TERM	C	AND I 3	2	1	0	AND B(I) 7	6	5	4	3	2	1	0	AND Q(P) 3	2	1	0	OR Q(N) 3	2	1	0	OR P B	A	OR R B	A	OR B(O) 7	6	5	4	3	2	1	0
0																																	
1																																	
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L_B																																	
L_A																																	
D7																																	
D6																																	
D5																																	
D4																																	
D3																																	
D2																																	
D1																																	
D0																																	
PIN		5	4	3	2	19	18	13	12	9	8	7	6	17	16	15	14																

FPLS PROGRAM TABLE (Logic)

82S156/157

PROGRAM TABLE ENTRIES:

C (AND)

INACTIVE	0
GENERATE	A
PROPAGATE	●
TRANSPARENT	–

(Q = J/K) (OR)

TOGGLE	0
SET	H
RESET	L
HOLD	–

I, Q, B(I) (AND)

INACTIVE	0
I, F, B	H
$\bar{I}$, $\bar{F}$, $\bar{B}$	L
DON'T CARE	–

P, R, B(O), (Q = D) (OR)

ACTIVE	A
INACTIVE	●

B(O) (POL.)

HIGH	H
LOW	L

F/F TYPE (OR)

J/K	●
D	A

NOTES
1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (–). Program unused Q, B, P, and R bits in the OR array as (–) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE ____

TERM	AND C	AND I 3	AND I 2	AND I 1	AND I 0	AND B(I) 5	AND B(I) 4	AND B(I) 3	AND B(I) 2	AND B(I) 1	AND B(I) 0	AND Q (P) 5	AND Q (P) 4	AND Q (P) 3	AND Q (P) 2	AND Q (P) 1	AND Q (P) 0	(F/F TYPE) OR Q (N) 5	OR Q (N) 4	OR Q (N) 3	OR Q (N) 2	OR Q (N) 1	OR Q (N) 0	OR P	OR R	(POLARITY) OR B(O) 5	OR B(O) 4	OR B(O) 3	OR B(O) 2	OR B(O) 1	OR B(O) 0
0																														
1																														
2																														
3																														
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L																														
D5																														
D4																														
D3																														
D2																														
D1																														
D0																														
PIN		5	4	3	2	19	12	9	8	7	6	18	17	16	15	14	13													

FPLS PROGRAM TABLE (Logic)

82S158/159

PROGRAM TABLE ENTRIES:

I, Q, B(I)

INACTIVE	O
I, F, B	H
$\overline{I}$, $\overline{F}$, $\overline{B}$	L
DON'T CARE	–

(AND)

C

INACTIVE	O
GENERATE	A
PROPAGATE	●
TRANSPARENT	–

(AND)

(Q = J/K)

TOGGLE	O
SET	H
RESET	L
HOLD	–

(AND)

$\overline{O.E.}$

IDLE	O
CONTROL	A
ENABLE	●
DISABLE	–

P, R, B(O), (Q = D)

ACTIVE	A
INACTIVE	●

(OR)

B(O)

HIGH	H
LOW	L

(POL.)

F/F TYPE

J/K	●
D	A

(OR)

NOTES
1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (–). Program unused Q and B bits in the OR array as (–) or (A), as applicable.
3. Unused Terms can be left blank.
4. If E_A = (0), E_B cannot be controlled, and vice versa.
5. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE ____

TERM	C	AND: I 3	I 2	I 1	I 0	B(I) 3	B(I) 2	B(I) 1	B(I) 0	Q (P) 7	Q (P) 6	Q (P) 5	Q (P) 4	Q (P) 3	Q (P) 2	Q (P) 1	Q (P) 0	($\overline{O.E.}$)	(E_B =)	(E_A =)	(POLARITY)	(OR): Q (N) 7	Q (N) 6	Q (N) 5	Q (N) 4	Q (N) 3	Q (N) 2	Q (N) 1	Q (N) 0	B(O) 3	B(O) 2	B(O) 1	B(O) 0
(F/F TYPE)																																	
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L_A																																	
D3																																	
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D1																																	
D0																																	
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12																

MILITARY

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES						
	CAN		DUAL-IN-LINE				
	8-PIN	10-PIN	8-PIN	14-PIN	16-PIN	18-PIN	24-PIN
PB	—	—	FE	—	—	—	—
CB	—	—	—	F	—	—	—
EB	—	—	—	—	F	—	—
JB	—	—	—	—	—	—	F
DB	—	—	—	W	—	—	—
FB	—	—	—	—	W	—	—
ZC	—	—	—	—	—	—	Q
GC	H	—	—	—	—	—	—
IC	—	H	—	—	—	—	—
VB	—	—	—	—	—	I	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	X	X	X
8T	—	X	X
93XX	X	X	X
96XX	—	X	X
Analog	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity or running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond.B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*
Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHDS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification						
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling* *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)	1010, Cond. C; (10 cycles, −65°C to +150°C)	100%	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30kg in Yl Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10−⁸CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ −55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard	10%	10% 3% Funct"l	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/ XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per pkg. group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constand acceleration.	Every 3 months per μcircuit type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

LOGIC—5400 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	—	—	F	—
5404	Hex Inverter	/00105	1	1	F	W
5411	Triple 3-Input AND Gate	—	—	—	F	W
5414	Hex Schmitt Trigger	/15102	—	—	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—
5432	Quad 2-Input OR Gate	/16101	1	1	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W
5443	Excess 3-to-Decimal Decoder	/01002	—	—	F	W
5444	Excess 3-Gray-to-Decimal Decoder	/01003	—	—	F	W
5446A	BCD-to-7 Segment Decoder/Driver	/01006	—	—	F	W
5447A	BCD-to-7 Segment Decoder/Driver	/01007	—	—	F	W
5453	4-Wide 2-Input AOI Gate (Expandable)	/00503	—	—	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W
5470	Dual D-Type Edge-Triggered Flip-Flop	/00205	—	—	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W
5477	Quad Bistable Latch	/01502	—	—	—	W
5416	4-Bit Binary Full Adder	/00602	—	—	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W
5491	8-Bit Shift Register	—	—	—	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W
5494	4-Bit Shift Register {PISO}	—	—	—	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W
54109	Dual J-K Positive Edge-Triggered Flip-Flop	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	1	—	F	W
54121	Monostable Multivibrator	/01201	1	1	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01203	1	1	F	W
54132	Quad Schmitt Trigger	/15103	1	1	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	—	—	F	W
54151	8-Line to 1-Line Mux	/01406	1	1	F	W
54152	8-Line to 1-Line Mux	—	—	—	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	1	1	F	W
54154	4-Line to 16-Line Decoder/Demux	/15201	1	—	F	W
54151	Quad 2-Input Data Selector {non-inv.}	/01405	1	1	F	W
54158	Quad 2-input Data Selector {inv.}	—	—	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	•	•	F	W
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	1	1	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	1	—	F	—
54190	Synchronous Up/Down Counter (BCD)	—	—	—	•	•
54191	Synchronous Up/Down Counter (Binary)	—	—	—	•	•
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	1	1	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	1	1	F	W
54279	Quad S-R Latch	—	—	—	F	W
54365A	Hex Buffer w/Common Enable (3-State)	/16301	1	—	F	R
54366A	Hex Buffer w/Common Enable (3-State)	/16302	1	—	F	R
54367A	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	1	—	F	R
54368A	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	1	—	F	R
9309	Dual 4 Input Multiplexer	/01404	1	1	F	W

NOTE
1 = QPLI 2 = QPLII • = In process

LOGIC—54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54LS00	Quad 2-Input NAND Gate	/30001	1	1	F	W
54LS02	Quad 2-Input NOR Gate	/30301	1	1	F	W
54LS04	Hex Inverter	/30003	1	1	F	W
54LS08	Quad 2-Input AND Gate	/31004	1	1	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W
54LS14	Hex Schmitt Trigger	/31302	1	1	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W
54LS28	Quad 2-Input NOR Buffer	/30204	—	—	F	W
54LS30	8-Input NAND Gate	/30009	—	—	F	W
54LS32	Quad 2-Input OR Gate	/30501	1	1	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	1	1	F	W
54LS42	BCD-to-Decimal Decoder	/30703	1	1	F	W
54LS51	Dual 2-Wide 2-Input A01 Gate	/30401	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	2	2	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	1	1	F	W
54LS75	Quad Bistable Latch	31601	2	2	F	W
54LS76	Dual J-K Master-Slave Flip-Flop	30110	1	1	F	W
54LS83A	4-Bit Binary Full Adder	/31201	—	—	F	W
54LS85	4-Bit Magnitude Comparator Gate	/31101	1	1	F	W
54LS86	Quad 2-Input Exclusive-OR Gate	/30502	1	1	F	W
54LS90	Decade Counter	/31501	1	1	F	W
54LS92	Divide-by-Twelve Counter	/31510	1	1	F	W
54LS93	4-Bit Binary Counter	/31502	1	1	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	1	1	F	W
54LS96	5-Bit Shift Register	/30604	1	1	F	W
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	1	1	F	W
54LS109	Dual J-K Positive Edge-Triggered Flip-Flop	/30109	1	1	F	W
54LS112	Dual J-K Negative Edge-Triggered Flip-Flop	/30103	1	1	F	W
54LS113	Dual J-K Negative Edge-Triggered Flip-Flop	/30104	1	1	F	W
54LS125	Quad Bus Buffer Gate w/3-State Outputs	/32301	1	1	F	W
54LS126	Quad Bus Buffer Gate w/3-State Outputs	/32302	1	1	F	W
54LS13	Quad Schmitt Trigger	/31303	—	—	F	W
54LS136	Quad Exclusive-or with o/c	—	—	—	F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	1	1	F	W
54LS139	Dual 2-to-4 Line Decoder/Demux	/30702	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	—	—	•	•
54LS153	Dual 4-Line to 1-Line Mux	/30902	1	1	F	W
54LS154	4-Line to 16-Line Decoder/Demux	—	—	—	1	Q
54LS156	Dual 2-Line to 4-Line Decode/Demux	/32602	2	2	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30903	—	—	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30904	—	—	F	W
54LS160A	Synchronous 4-Bit Decade Counter	/31503	•	•	F	W
54LS161A	Synchronous 4-Bit Binary Counter	/31504	•	•	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	—	—	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	1	1	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	1	1	F	W
54LS173	Quad D-Type Flip-Flop (3-State) (8T10)	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	1	1	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	1	1	F	W
54LS181	4-Bit Arithmetic Logic Unit	/30801	1	—	F	W
54LS190	Synchronous Up/Down Counter (BCD)	/31513	1	1	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	1	1	F	W

NOTE
1 = Level 1 Qualification 2 = Level 2 Qualification = In process

OGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54LS192	Synchronous Decade Up/Down Counter	/31507	•	•	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	1	1	F	W
54LS194A	4-Bit Bidirectional Universal Shift Register	/30601	—	—	F	W
54LS195A	4-Bit Parallel-Access Shift Register	/30602	1	1	F	W
54LS197	Presettable Binary Counter/Latch (8291)	/32002	•	•	F	W
54LS221	Dual Monostable Multivibrator	/31402	—	—	•	•
54LS240	Octal Inverter Buffer 3-State	/32401	•	—	F	—
54LS241	Octal Buffer 3-State	/32402	•	—	F	—
54LS242	Quad Inverting TCRS. 3-State	/32801	•	•	F	W
54LS243	Quad TCRS. 3-State	/32802	•	•	F	W
54LS244	Octal Buffer 3-State	/32403	•	—	F	—
54LS245	Octal TCRS. 3-State	/32803	•	—	F	—
54LS251	Data Selector/Mux with 3-State Outputs	/30905	—	—	•	•
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30908	—	—	F	W
54LS257A	Quad 2-Line to 1-Line Data Selector/Mux	/30906	1	1	•	•
54LS258A	Quad 2-Line to 1-Line Data Selector/Mux	/30907	1	1	•	•
54LS260	Dual 5-Input NOR Gate	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	/31801	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	1	1	F	W
54LS273	Octal D. Flip Flop	/32501	2	•	F	W
54LS279	Quad S-R Latch	/31602	•	•	F	W
54LS283	4-Bit Adder	/31202	—	—	F	W
54LS290	Decade Counter	/32003	1	1	F	W
54LS293	4-Bit Binary Counter	/32004	1	1	F	W
54LS295B	4-Bit Right-Shift Left-Shift Register	/30606	1	1	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	F	W
54LS365	Hex Buffer w/common Enable (3-State)	/32201	1	1	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	—	—	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	1	1	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	1	1	F	W
54LS373	Octal Transparent Latch (3-State)	/32502	•	—	F	—
54LS374	Octal D Flip Flop (3-State)	/32503	—	—	F	—
54LS375	Quad Latch	—	—	—	F	W
54LS377	Octal D Flip Flop Clock Enable	/32504	—	—	F	—
54LS395A	4-Bit Cascadeable Shift Register (3-State)	/30607	1	1	F	W
54LS670	4X4 Register File (3-State)	/31901	—	—	F	W

OTE
=Level 1 Qualification
=Level 2 Qualification
=in Process

LOGIC—54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W
54S02	Quad 2-Input NOR Gate	/07301	1	1	F	W
54S04	Hex Inverter	/07003	1	1	F	W
54S08	Quad 2-Input AND Gate	/08003	1	1	F	W
54S10	Triple 3-Input NAND Gate	/07005	1	1	F	W
54S11	Triple 3-Input NAND Gate	/08001	1	1	F	W
54S15	Triple 3-Input AND Gate with o/c	/08002	—	—	F	W
54S20	Dual 4-Input NAND Gate	/07006	—	—	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—
54S40	Dual 4-Input NAND Buffer	/07201	1	1	F	W
54S51	Dual 2-Wide 2-Input A01 Gate	/07401	1	1	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	1	1	F	W
54S85	4-Bit Magnitude Comparator	/08201	1	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/07501	1	1	F	W
54S112	Dual J-K Negative Edge-Triggered Flip-Flop	/07102	1	1	F	W
54S113	Dual J-K Negative Edge-Triggered Flip-Flop	/07103	2	2	F	W
54S133	13-Input NAND Gate	/07009	1	1	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—
54S138	3-to-8 Line Decoder/Demux	/07701	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/Demux	/07702	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	1	1	F	W
54S151	8-Line to 1-Line Mux	/07901	1	1	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	1	1	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	1	1	F	W
54S158	Quad 2-Input Data Selector (inv)	/07904	1	1	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07105	—	—	F	W
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07106	—	—	—	—
54S181	4-Bit Arthmetic Logic unit	/07801	1	—	F	*
54S182	Look-Ahead Carry Generator	/07802	—	—	*	*
54S194	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—
54S195	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—
54S251	Data Selector/Mux with 3-State Outputs	/07905	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—
54S258	Quad 2-Line to 1-Line Data Selector/Mux	/07907	—	—	—	—
54S260	Dual 5-Input NOR Gate	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—

NOTE

Per QPL 38510-32 dated
10 January 1978
1=Level 1 Qualification
2=Level 2 Qualification
*=In Process

LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL-STD 883	
			DIP	FLAT-PACK
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T09	Quad Bus Driver with 3-State Outputs	—	F	W
8T13	Dual Line Driver	—	F	W
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	—	F	W
8T22	Retriggerable Monostable Multivibrator (54122/9601)	—	F	W
8T26A	Quad Bus Driver/Receiver (3-State Outputs)	—	F	R
8T28	Quad Non-Inverting Bus Driver/Receiver (3-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	•	•
8T32	Programmable 8-Bit, I/O Port (3-State), IV Byte	—	I	•
8T33	Programmable 8-Bit, I/O Port (Open Collector), IV Byte	—	I	•
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)		I	W
8T37	Hex Bus Receiver with Hysteresis-Schmitt Trigger		F	W
8T38	Quad Bus Transceiver (Open Collector) (DM8838)		F	W
8T80	Quad 2-Input NAND Gate (High Voltage)		F	W
8T90	Hex Inverter (High Voltage)	—	F	W
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	R
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)		F	R
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)		F	R
8T126	Quad 3-State Transceivers	—	F	W
8T127	Quad 3-State Transceivers	—	F	W
8T128	Quad 3-State Transceivers	—	F	W
8T129	Quad 3-State Transceivers	—	F	W

• = Qualification planned

BIPOLAR MEMORY

DEVICE	ORGANIZATION	PACKAGE*		OUTPUT CIRCUIT	NUMBER OF PINS
PROMs					
82S23	32X8	F	R	OC	16
82S115	512X8	I	R	TS	24
82S123	32X8	F	W	TS	16
82S126	256X4	F	W	OC	16
82S129	256X4	F	R	TS	16
82S130	512X4	F	R	OC	16
82S131	512X4	F	R	TS	16
82S137	1024X4	F,I	R	TS	18
82S141	512X8	F,I	R	TS	24
82S181	1024X8	F,I	R,G	TS	24
82LS181	1024X8	F	R	TS	24
82S185	2048X4	I	R	TS	18
82S2708	1024X8	F,I	R	TS	24
82LS2708	1024X8	F	R	TS	24
82S191	2048X8	I	R,G	TS	24
FPLF					
82S100	16X48X8	I	R,G	TS	28
82S101	16X48X8	I	R	OC	28
82S102	16X9	I	R	OC	28
82S103	16X9	I	R	TS	28
82S106	16X48X8	I	R	OC	28
82S107	16X48X8	I	R	OC	28
PLAs					
82S200	16X48X8	I	R	TS	28
82S201	16X48X8	I	R	OC	28
RAMs					
54S189	16X4	F	R	TS	16
54S301	256X1	F	R	OC	16
82S09	64X9	I	R	OC	28
82S19	64X9	I	R	OC	28
82S16	256X1	F	R	TS	16
82S25	16X4	F	R	OC	16

R = BeO Flat Pack
F = Cerdip
I = Ceramic DIP
G = Leadless 28 PINS
W = Ceramic Flat Pack

JAN M-38510			
DEVICE	SLASH SHEET	PKG	QUAL STATUS
82S23	/20701	F	QPL II
82S123	/20702	F	QPL II
82S126	/20301	F	QPL I
82S129	/20302	F	QPL I
82S130	/20401	F	QPL II
82S131	/20402	F	QPL I
82S137	/20602	F	QPL II
82S141	/20802	F	QPL II
82S115	/20803	F	QPL II
82S181	/20904	F	QPL II
82S185	/20902	I	QPL II
82S2708	/20905	I	QPL II
82S191	/21002	I	QPL II
82S100	/ (Draft)	I	Planned

+ Per QPL M38510-38 dated June 1980

BIPOLAR MEMORY CROSS REFERENCE

AMD	SIGNETICS
2700/27LS00	82S16
27S08/27LS08	82S23
27S09/27LS09	82S123
27S10	82S126
27S11	82S129
3101	82S25

FAIRCHILD	SIGNETICS
93403	82S25
93417	82S126
93419	82S09
93421	82S16
93427	82S129
93431	82S130
93436	82S130
93441	82S131
93446	82S131
93448	82S141
93453	82S137
93457	82S126
93467	82S129
93451	82S181
——	82S191

HARRIS	SIGNETICS
0064	82S25
HM7602-2	82S23
HM7603-2	82S123
HM7608-2	82S2708
HM7610-2	82S126
HM7611-2	82S129
HM7620-2	82S130
HM7621-2	82S131
HM7641-2	82S141
HM7643-2	82S137
HM7647-2	82S115
HM7681-2	82S181
HM7685-2	82S185
HM76161	82S191

INTEL	SIGNETICS
2708	82S2708
3101	82S25
3106/A	82S16
3601	82S126
3602	82S130
3605	82S136
3622	82S131
3624	82S141
3625	82S137
3628	82S181
3636	82S191

INTERSIL	SIGNETICS
5501	82S25
5523A	82S16
5533	54S301
5600	82S23
5603A	82S126
5604	82S130
5610	82S123
5623A	82S129
5624	82S131
5625	82S141
56526	82S137

MOTOROLA	SIGNETICS
4064	82S25
4256	82S16
5005	82S126

MMI	SIGNETICS
5300-1	82S126
5301-1	82S129
5305-1	82S130
5306-1	82S131
5330	82S23
5331	82S123
5341	82S141
5353	82S137
5381	82S181
5385	82S2708
5531	82S16
5560	82S25

NATIONAL	SIGNETICS
54S188	82S23
54S287	82S129
54S288	82S123
54S387	82S126
54S570	82S130
54S571	82S131
54S573	82S137
86L99	82S25
87S296	82S141
87S181	82S181
87S191	82S191

T.I.	SIGNETICS
54S188	82S23
54S189	54S189
54S287	82S129
54S288	82S123
54S301	54S301
54S387	82S126
54S474	82S141
54S476	82S137
54S478	82S181

NOTE

Parts are pin for pin functional replacements except where noted.

LINEAR DEVICES

DEVICE	DESCRIPTION	PACKAGE*	
		DIP	CAN
	OPERATIONAL AMPLIFIERS		
LF155	JFET Op Amp		H
LF156	JFET Op Amp		H
LH2101A	Dual Op Amp	F	
LM101/A	Hi Perf Op Amp	F	H
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		H
MC1556	Hi Perf Op Amp	F	H
MC1558	Dual Op Amp	F	H
SE530	Hi Slew Op Amp	F	H
SE532	Dual Op Amp		H
SE5512	Dual Op Amp	FE	H
SE5532	Dual Op Amp	F,FE	H
SE5532A	Dual Op Amp	FE	
SE5534	Lo Noise Op Amp	F,FE	H
SE5534A	Lo Noise Op Amp	FE	H
SE5537	Sample and Hold Amp	FE	H
SE5539	High Freq Op Amp	F	—
μA747	Dual Op Amp	F	H
	COMPARATORS		
SE521	Dual Differential Comparator	F	
SE522	Dual Differential Comparator	F	
SE527	Voltage Comparator	F	H
SE529	Voltage Comparator	F	H
LH2111	Dual Voltage Comparator	F	
LM111	Voltage Comparator	F	H
LM139/A	Quad Voltage Comparator	F	
LM193/A	Dual Voltage Comparator		H
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
μA733	Video Amplifier	F	H
	PHASE LOCKED LOOPS		
SE567	Tone Decoder PLL	F	H
SE564	Phase Locked Loop	F	H
	TIMERS		
SE555	Timer	F,FE	H
SE556-1	Dual Timer	F	
SE558	Quad Timer	F	

DEVICE	DESCRIPTION	PACKAGE*	
		DIP/CAN	CAN
	VOLTAGE REGULATORS		
SE5553	Dual Track Reg	F	H
SE5554	Dual Track Reg	F	H
μA723	Adj Volt Reg	F	H

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	D to A CONVERTERS		
DAC-08	8-Bit Mult DAC	F,Q	H
MC1508-8	8-Bit Mult DAC	F	—
SE5008	8-Bit Mult DAC	F	—
SE5009	8-Bit Mult DAC	F	—
SE5018	8-Bit μP-Comp DAC	F	—
SE5019	8-Bit μP-Comp DAC	F	—
SE5118	8-Bit μP-Comp DAC	F	—
SE5119	8-Bit μP-Comp DAC	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	DUAL LINE RECEIVERS		
DS7820/A	Dual Line Receiver	F	—
DS7830/A	Dual Diff Line Driver	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	MOS FET SWITCH		
SD210	Switch N-Channel Enhance	EE	—
SD211	Switch N-Channel Enhance	EE	—
SD5002	Quad Analog Switch	I	

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	SMPS CONTROL CIRCUITS		
SE5560	SMPS Controller	F	—
SG1524	Reg Pulse Width Mod	F	—

JAN M – 38510			
DEVICE	SLASH SHEET	PKG	QUAL STATUS
SE555	10903BCB	F	QPL 1
SE555	10903BPB	FE	QPL 1
SE555	10901BGC	H	QPL 1
SE556-1	10902BCB	F	QPL 1
LH2101A	10105BEB	F	QPL 1
LM101A	10103BCB	F	QPL 1
LM101A	10103BPB	FE	QPL 1
LM101AH	10103BGC	H	QPL 1
μA741	10101BGC	H	QPL 1
μA747	10101BGC	H	QPL 1
LM124	11005BCB	F	1980
DAC-08	11301BCB	F	1980
DAC-08A	11302BCB	F	1980
SE5537			1980
SG1524			1980

NOTES
F = Cerdip
H = TO-5

LINEAR INDUSTRY CROSS REFERENCE

FAIRCHILD	SIGNETICS
μA111	LM111
μA139	LM139
μA733	μA733
μAF155/156	LF155/156
μA101	LM101
μA101A	LM101A
MC1556	MC1556
μA1558	MC1558
μA747	μA747
MC1555	SE555
μA556	SE556
μA109	LM109
μA79XX	79XX(7)
μA723	μA723

MOTOROLA	SIGNETICS
MLM111	LM111
MC1733	μA733
LF155/56	LF155/156
MLM101	LM101
MLM101A	LM101A
MC1558	MC1558
MC1747	μA747
MC3556	SE556
MLM109	LM109
MC78XX	78XX(7)
MC79XX	79XX(7)
MC1723	μA723
MC1508	MC1508-8

NATIONAL	SIGNETICS
LM161	SE527
LH2111	LH2111
LM111	LM111
LM119	LM119
LM139	LM139
LM193	LM193/193A
LM733	μA733
LF155/56	LF155/156
LH2101A	LH2101A
LH2108A	LH2108A
LM101A	LM101
LM101	LM101A
LM124	LM124
LM158	LM158
LM1558	MC1558
LM1581	SE532
LM747	μA747
LM567	SE567
DM7820	DM7820
DM7830	DM7830
LM555	SE555
LM109	LM109
LM723	μA723

PMI	SIGNETICS
SSS1508	MC1508-8
DAC-08	SE5008

RAYTHEON	SIGNETICS
LM111	LM111
LM139	LM139
RM733	μA733
LF155/56/57	LF155/156
LM101	LM101
LM101A	LM101A
LM124	LM124
RM1556	MC1556
RM1558	MC1558
RM747	μA747
RM555	SE555
LM109	LM109
RM723	μA723

T.I.	SIGNETICS
LM111	LM111
SN52733	μA733
LF155/56	LF155/156
SN52101A	LM101A
SN55182	DM7820
SN55183	DM7830
SN52555	SE555
SE556	SE556
LM109	LM109
μA79XX	μA79XX(7)
SN52723	μA723

BIPOLAR MICROPROCESSORS

PRODUCT	DESCRIPTION	AVAILABILITY	
		DIP	FLAT PACK
3001	Microprogram Control Unit	I	R
3002	Central Processing Element (2-bit slice)	I	R
8X300	Interpreter/Microcontroller	I	•

• Under development

MICROPROCESSOR SUPPORT CIRCUITS

PRODUCT	DESCRIPTION	AVAILABILITY	
		DIP	FLAT PACK
LOGIC			
54123	Retriggerable Monostable Multivibrator	F	R
54180	8-Bit Odd/Even Parity Checker	F	R
54LS194	4-Bit Bidirectional Shift Register	I	•
54LS195	4-Bit Parallel Access Shift Register	I	•
54LS365	High Speed Hex 3-State Buffer	F	W
54LS366	High Speed Hex 3-State Buffer	F	W
54LS367	High Speed Hex 3-State Buffer	F	W
54LS368	High Speed Hex 3-State Buffer	F	W
	INTERFACE		
8T09	Quad Bus Driver with 3-State Output	F	W
8T13	Dual Line Driver	F	W
8T26A	Quad Bus Driver/Receiver (3-State)	F	W
8T28	Quad Bus Non-Inverting Driver/Receiver (3-State)	F	W
8T32	Programmable 8-Bit I/O Port (3-State), IV Byte	I	•
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	I	•
8T95	High Speed Hex Buffer (3-State)	F	R
8T97	High Speed Hex Buffer (3-State)	F	R
8T98	High Speed Hex Inverter (3-State)	F	R
8T126	Quad 3-State Transceivers	F	W
8T127	Quad 3-State Transceivers	F	W
8T128	Quad 3-State Transceivers	F	W
8T129	Quad 3-State Transceivers	F	W

• Under development

CHIP PROGRAM

Signetics is currently a major supplier of chips to both the Military / Aerospace and Commercial marketplaces. All chip and wafer sales are processed through Military Products Division.

To further enhance Signetics' ability to service the chip marketplace, Signetics has appointed distributors to stock and resell our full line of integrated circuit chips.

Our distributors can be contacted at the following address:

Hybritek Ltd.,
125, Long Lane
Chadderton
Lancashire OL9 8AY
England

Tel: 061-681-6658/061-682-6575

(Telex 666726)

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminature packages.
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

Hermetic Only

10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb .010 inches.
16. Maximum glass climb or lid skew is .010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc}(°C/W)	DESCRIPTION[1]
Standard Dual-In-Line			
8	NE	162/65	
14	NH	150/65	TO-116/MO-001
16	NJ	137/53	MO-001
18	NK	135/53	
20	NL	135/53	
22	NM	120/53	
24	NN	116/53	MO-015
24	NNE NNF	120/60	Slim Line
28	NQ	116/53	MO-015
40	NW	110/50	MO-015
Power Dual-In-Line			
14	NHA[2]	95/33	Butterfly
16	NJA[2]	95/33	Butterfly
18	NKA[2]	90/26	Butterfly
20	NLA[2]	90/26	Butterfly
24	NNA[2]	60/23	Heatsink
28	NQA[2]	56/21	Heatsink
SO Packages			
8	DE	110	SO-8
14	DH	100	SO-14
16	DJ	100	SO-16

NOTES
1. Dual-in-Line packages unless otherwise described.
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads.

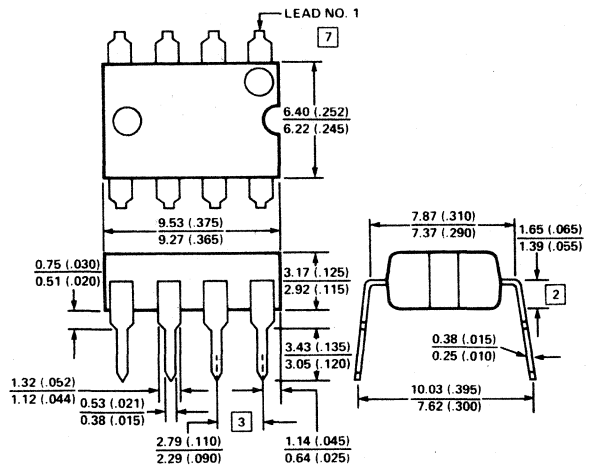
HERMETIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc}(°C/W)	DESCRIPTION[1]
Metal Headers			
3	HBA	100/20	TO-5 Header
4	EC	100/20	TO-46 Header
4	EE	150/25	TO-72 Header
8	HEA/HEB	150/25	TO-5 Header
10	HFB/HFA	150/25	TO-5/TO-100 Header, Short Can
10	HFD/HFC	150/25	TO-5/TO-100 Header, Tall Can
Flat Packs			
10	QF	230/55	Flat Ceramic
10	WF	240/50	Flat Ceramic
14	QHA	185/45	Flat Ceramic Laminate
14	WH	205/50	Flat Ceramic
16	QJA	170/45	Flat Ceramic Laminate
16	RJA	133/30	Flat Ceramic, BeO
16	WJ	200/50	Flat Ceramic
18	RKA	107/22	Flat Ceramic, BeO
24	QNA	155/44	Flat Ceramic Laminate
24	RNA	107/22	Flat Ceramic, BeO
24	WN	155/40	Flat Ceramic
28	RQA	107/22	Flat Ceramic, BeO
40	RWA	95/20	Flat Ceramic, BeO
Cerdip Family			
8	FE	110/30	Dual-in-Line Ceramic
14	FH	110/30	Dual-in-Line Ceramic
16	FJ	100/30	Dual-in-Line Ceramic
18	FK	93/27	Dual-in-Line Ceramic
20	FL	90/25	Dual-in-Line Ceramic
22	FM	75/27	Dual-in-Line Ceramic
24	FN	60/26	Dual-in-Line Ceramic
28	FQ	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
8	IEA	100/30	Dip Laminate
14	IHA	95/25	Dip Laminate
16	IJA	90/25	Dip Laminate
18	IKA/IKB	88/25	Dip Laminate
22	IMA	80/25	Dip Laminate
24	INC/INH	65/25	Dip Laminate
28	IQA	60/25	Dip Laminate
28	GQ*	90/35	Chip Carrier
40	IWA	55/25	Dip Laminate
44	GX*	75/30	Chip Carrier
48	JY*	55/25	Dual-in-Line Ceramic
50	IZA	42/20	Dip Laminate

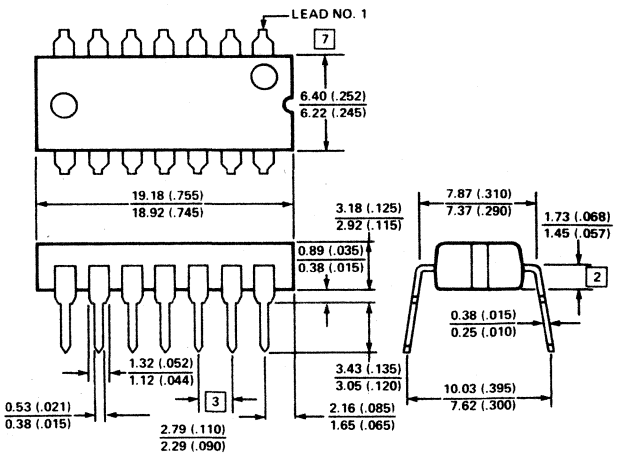
*Contact factory for Package drawings.

PLASTIC: Standard and Power Dual-In-Line

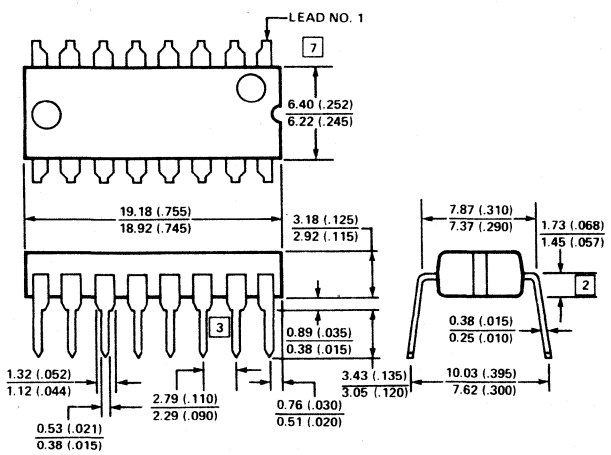
NE Package



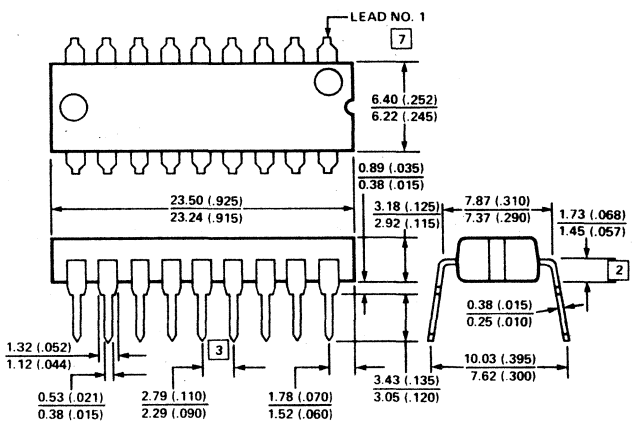
NH Package



NJ Package

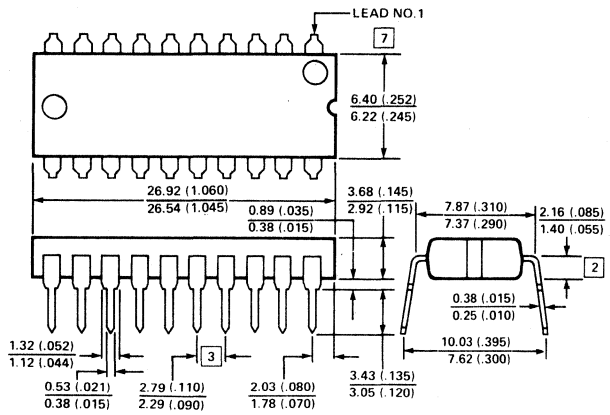


NK Package

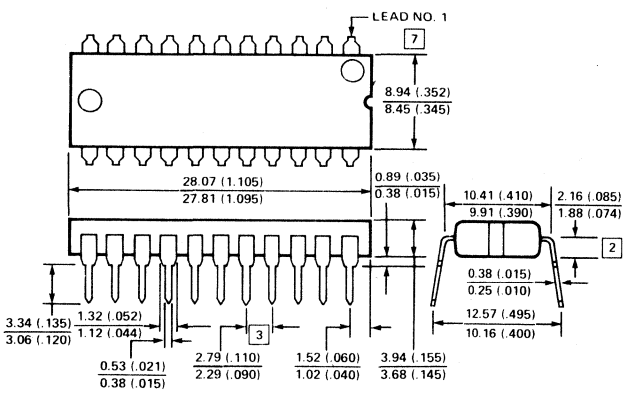


PLASTIC: Standard and Power Dual-In-Line (cont'd.)

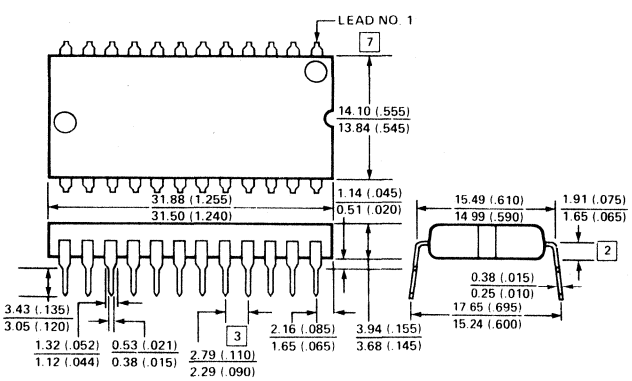
NL Package



NM Package

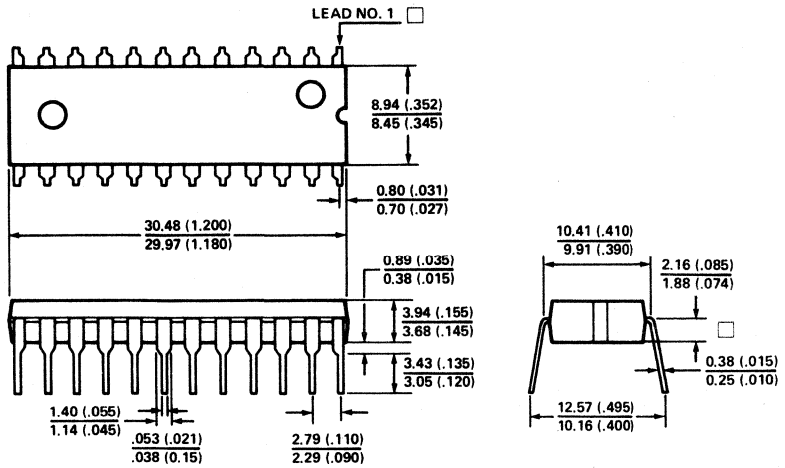


NN Package

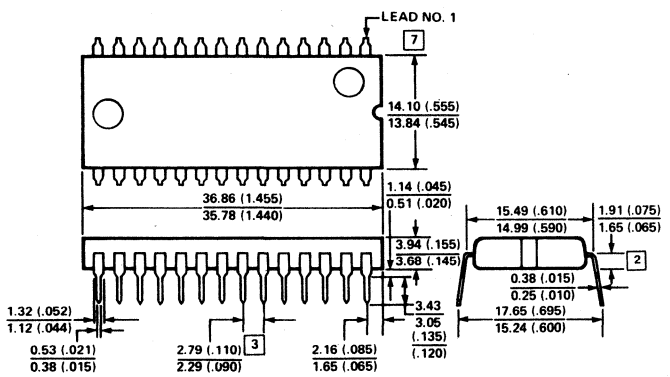


PLASTIC: Standard and Power Dual-In-Line (cont'd.)

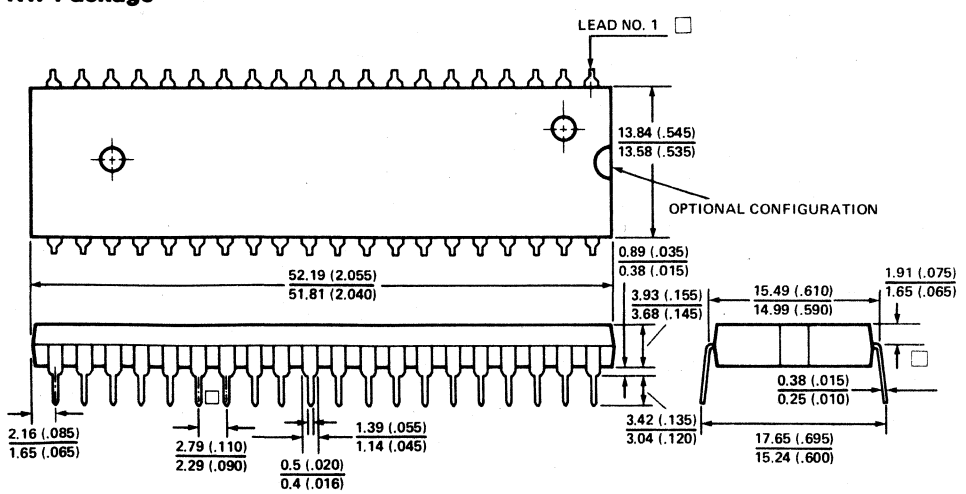
NNE/NNF Package



NQ Package

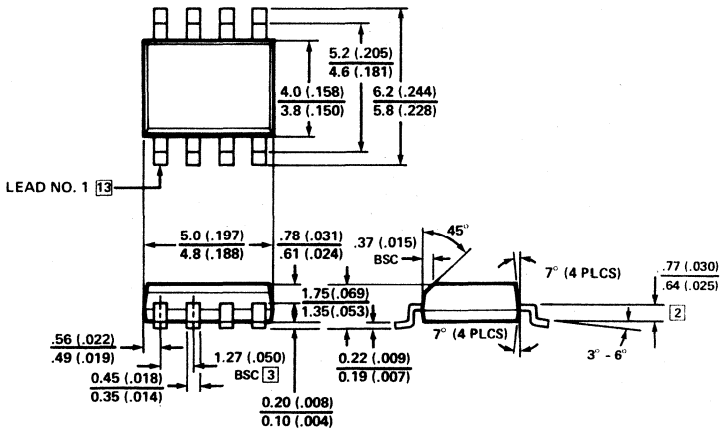


NW Package

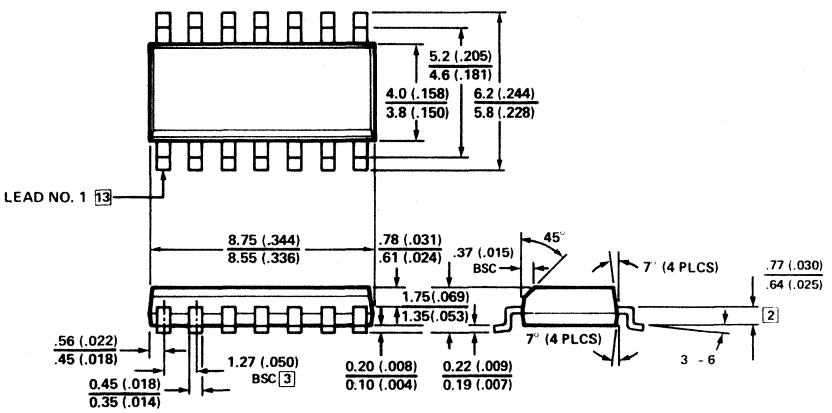


PLASTIC: SO Packages

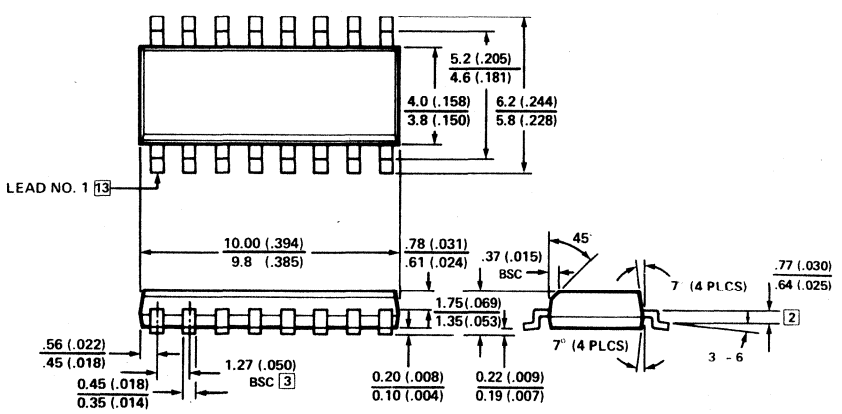
DE Package



DH Package

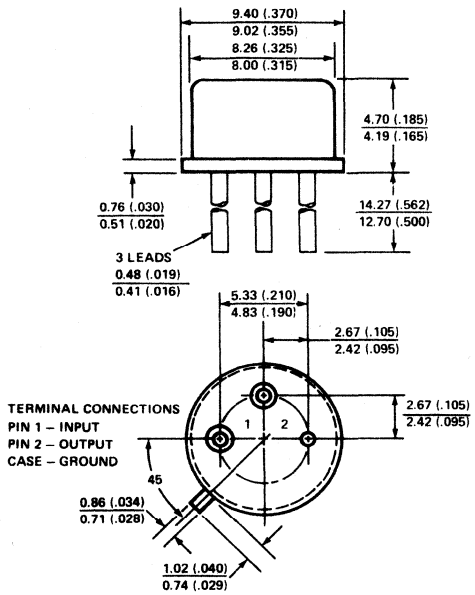


DJ Package



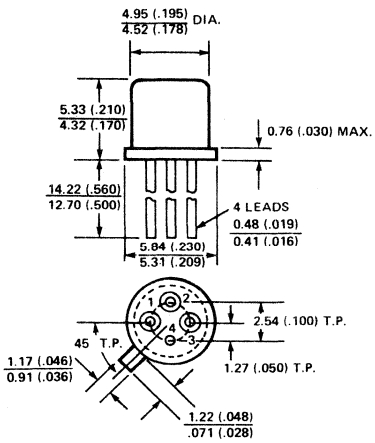
HERMETIC: Metal Headers

HBA Package



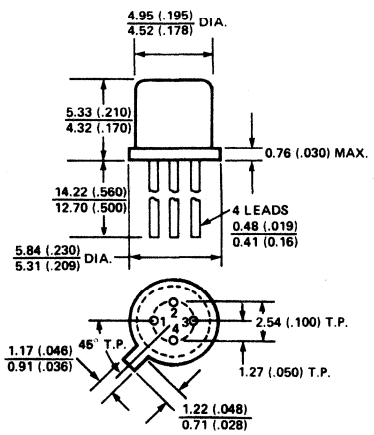
CONSTRUCTION NOTES: 10a, 11a, 12a

EC Package



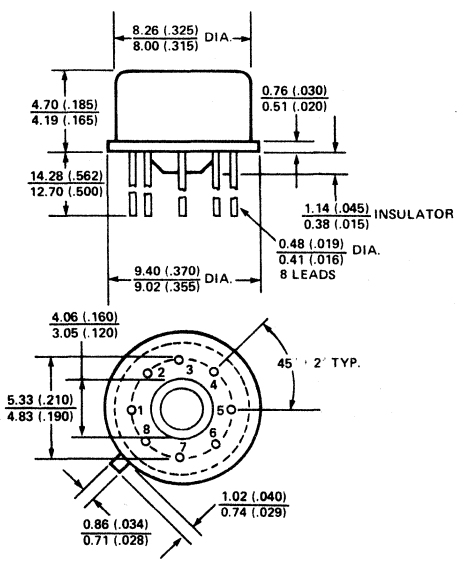
CONSTRUCTION NOTES: 10a, 11a, 12a

EE Package



CONSTRUCTION NOTES: 10a, 11a, 12a

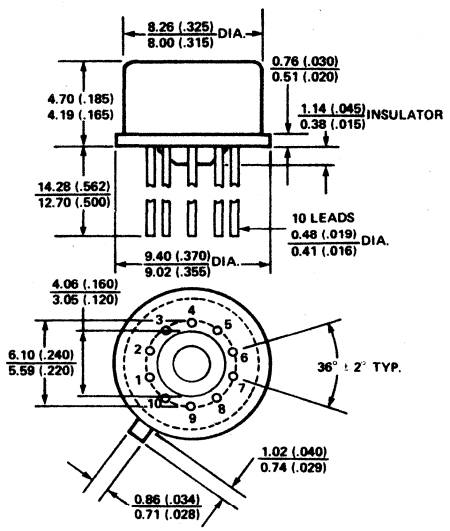
HEA/HEB Package



CONSTRUCTION NOTES: 10a, 11a, 12a

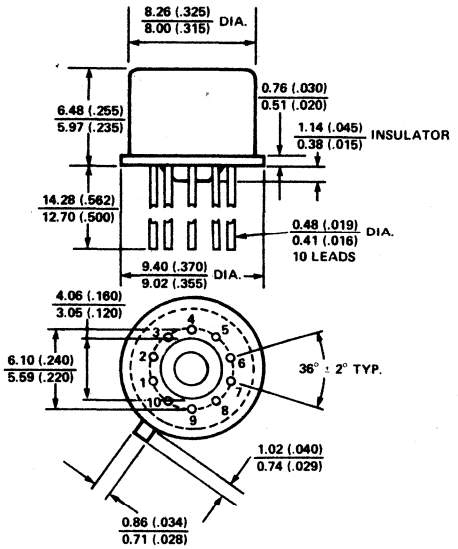
HERMETIC: Metal Headers (cont'd.)

HFB/HFA Package



CONSTRUCTION NOTES: 10a, 11a, 12a

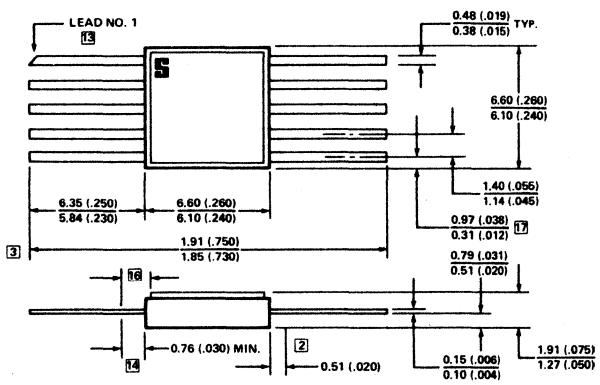
HFD/HFC Package



CONSTRUCTION NOTES: 10a, 11a, 12a

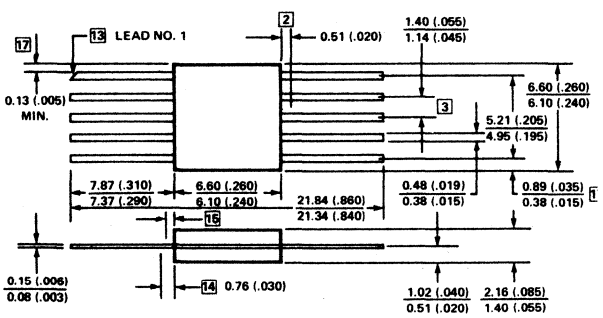
HERMETIC: Flat Packs

QF Package



CONSTRUCTION NOTES: 10c, 11d, 12b

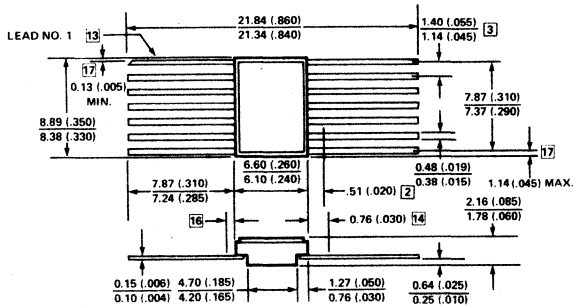
WF Package



CONSTRUCTION NOTES: 10b, 11b, 12b

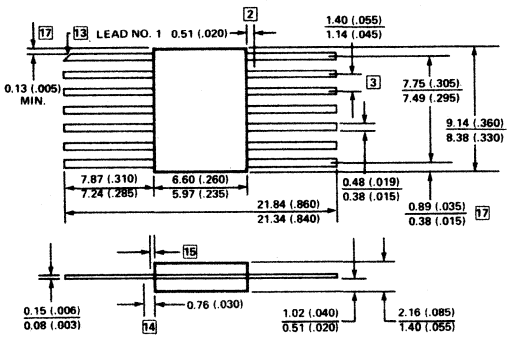
HERMETIC: Flat Packs (cont'd.)

QHA Package



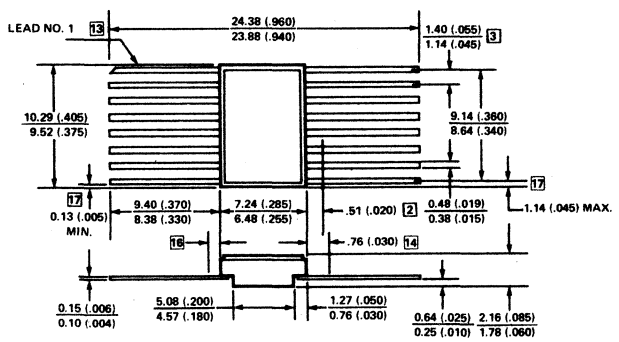
CONSTRUCTION NOTES: 10c, 11d, 12b

WH Package



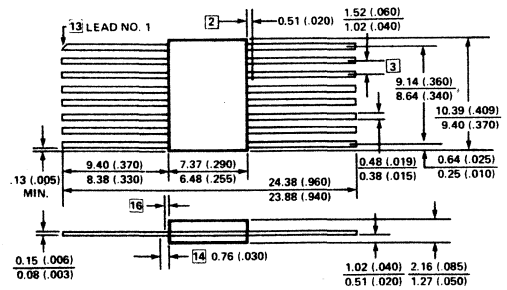
CONSTRUCTION NOTES: 10b, 11b, 12b

QJA Package



CONSTRUCTION NOTES: 10c, 11d, 12b

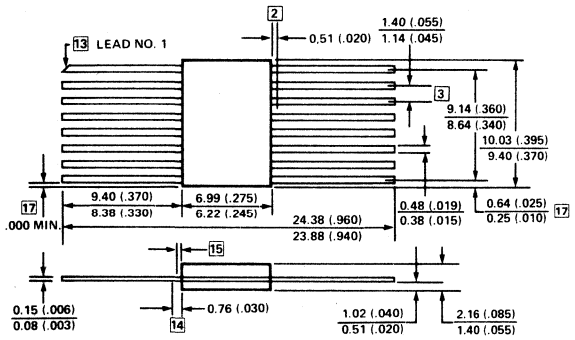
RJA Package



RJA CONSTRUCTION NOTES: 10b, 11c, 12b

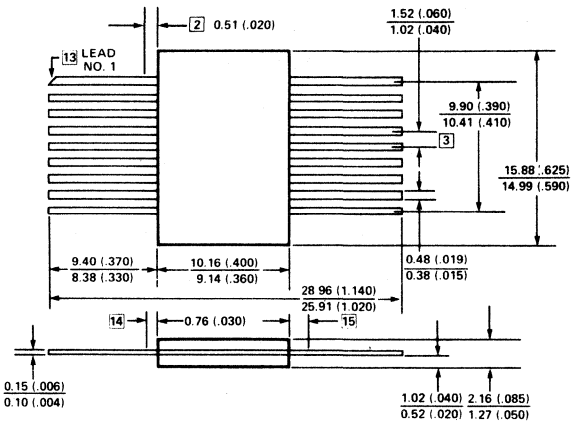
HERMETIC: Flat Packs (cont'd.)

WJ Package



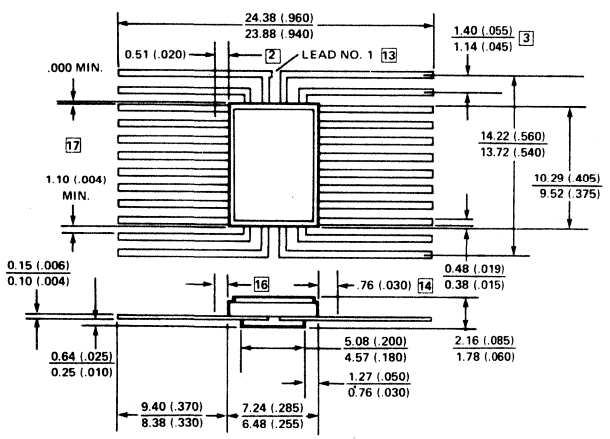
CONSTRUCTION NOTES: 10b, 11b, 12b

RKA Package



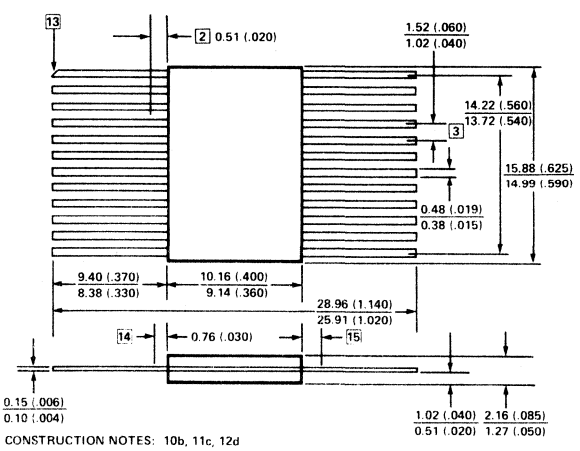
CONSTRUCTION NOTES: 10b, 11c, 12d

QNA Package



CONSTRUCTION NOTES: 10c, 11d, 12b

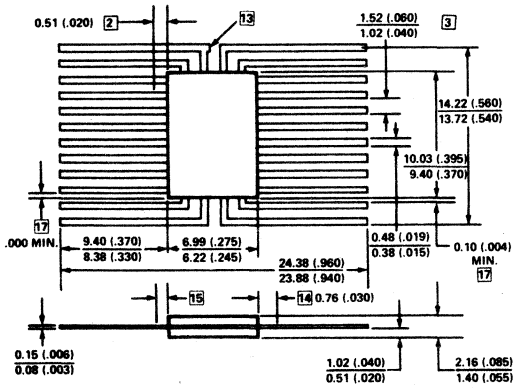
RNA Package



CONSTRUCTION NOTES: 10b, 11c, 12d

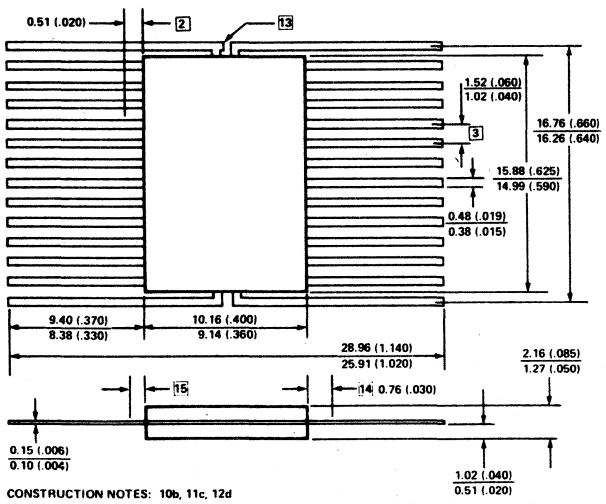
HERMETIC: Flat Packs (cont'd.)

WN Package



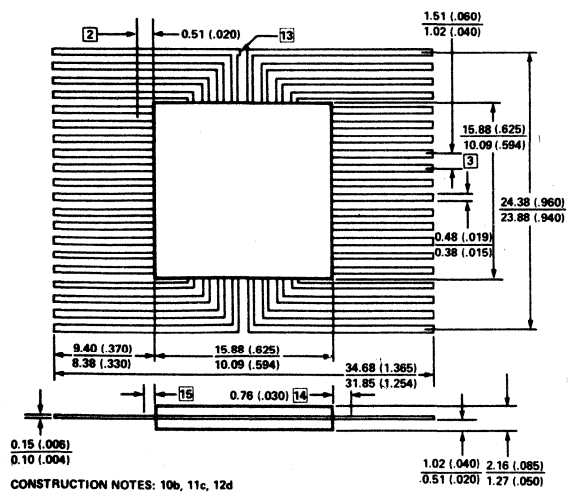
CONSTRUCTION NOTES: 10b, 11b, 12b

RQA Package



CONSTRUCTION NOTES: 10b, 11c, 12d

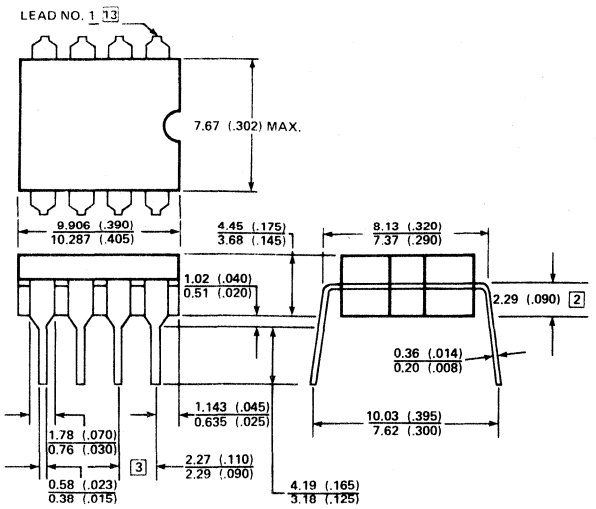
RWA Package



CONSTRUCTION NOTES: 10b, 11c, 12d

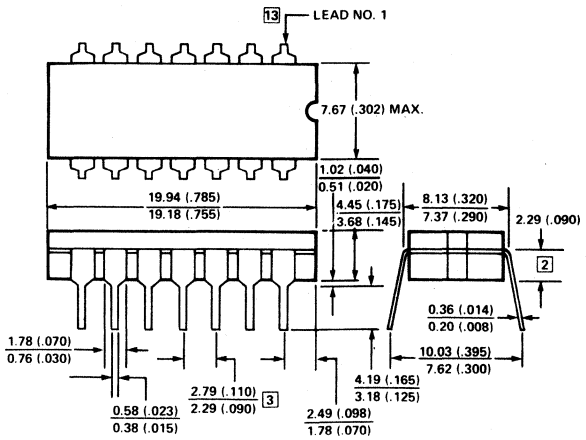
HERMETIC: Cerdip Family

FE Package



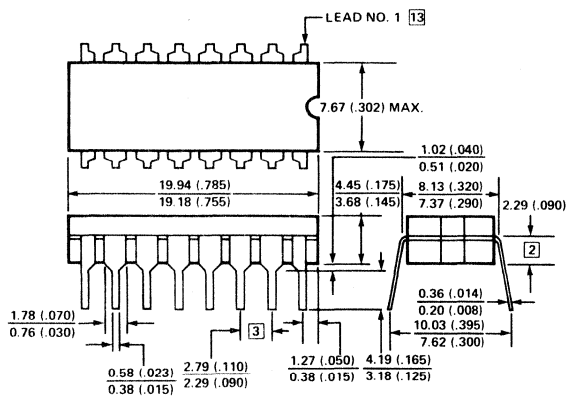
CONSTRUCTION NOTES: 10b, 11b, 12b

FH Package



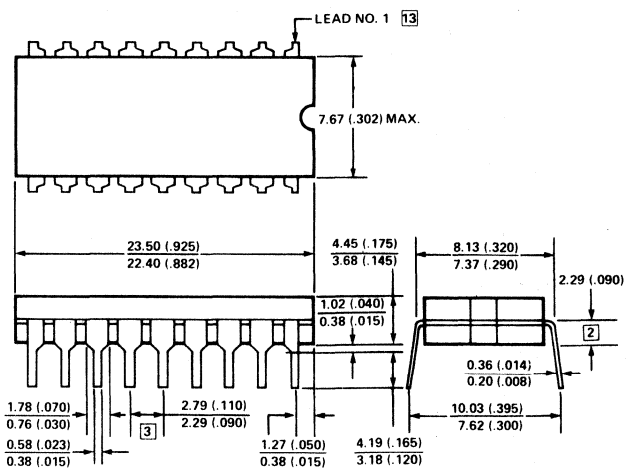
CONSTRUCTION NOTES: 10b, 11b, 12b

FJ Package



CONSTRUCTION NOTES: 10b, 11b, 12b

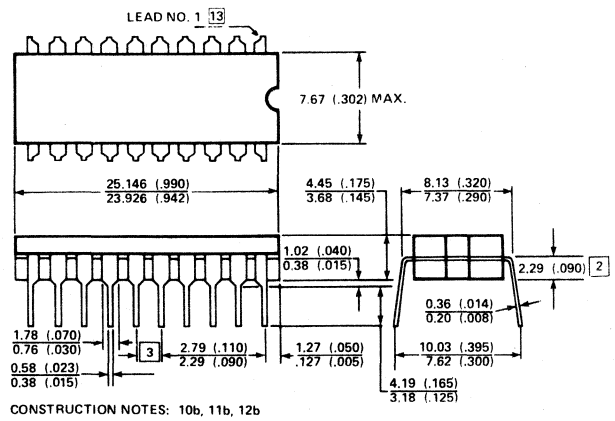
FK Package



CONSTRUCTION NOTES: 10b, 11b, 12b

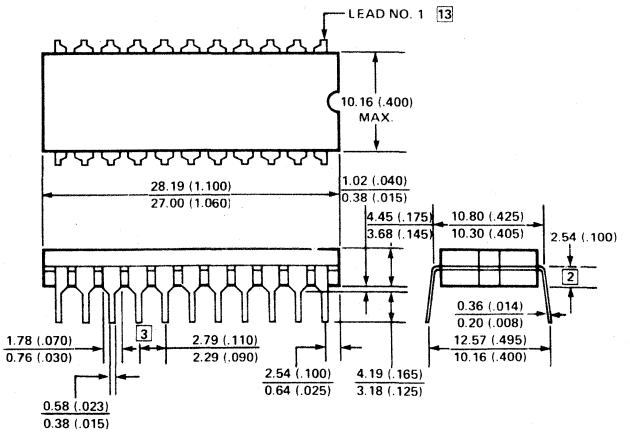
HERMETIC: Cerdip Family (cont'd.)

FL Package



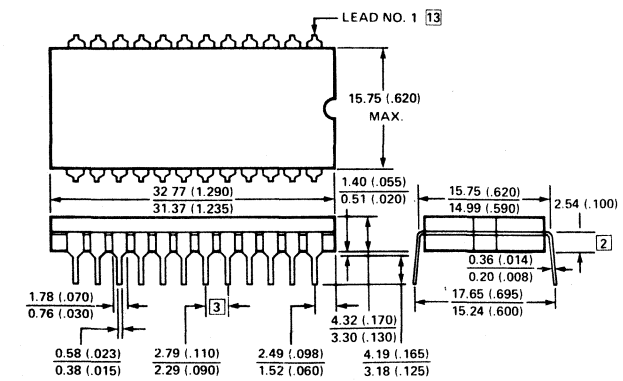
CONSTRUCTION NOTES: 10b, 11b, 12b

FM Package



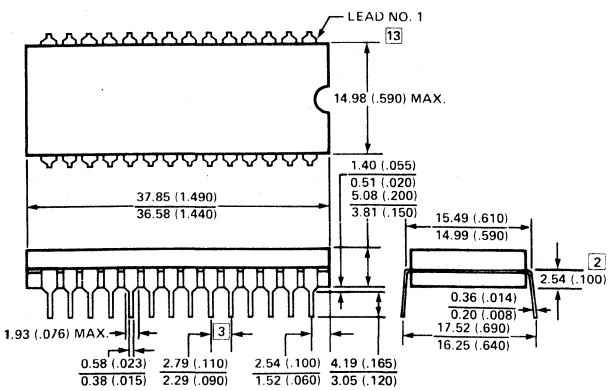
CONSTRUCTION NOTES: 10b, 11b, 12b

FN Package



CONSTRUCTION NOTES: 10b, 11b, 12b

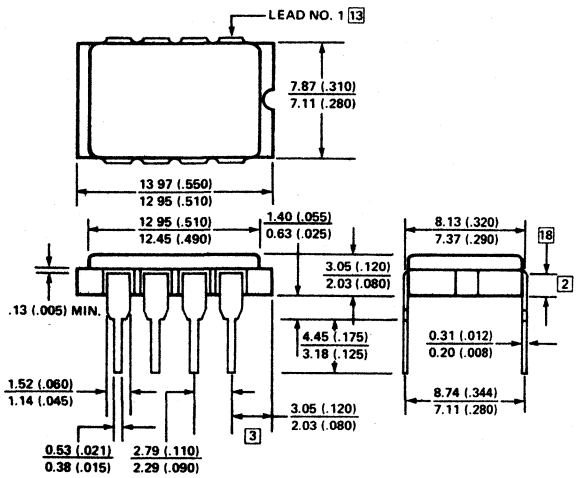
FQ Package



CONSTRUCTION NOTES: 10b, 11b, 12b

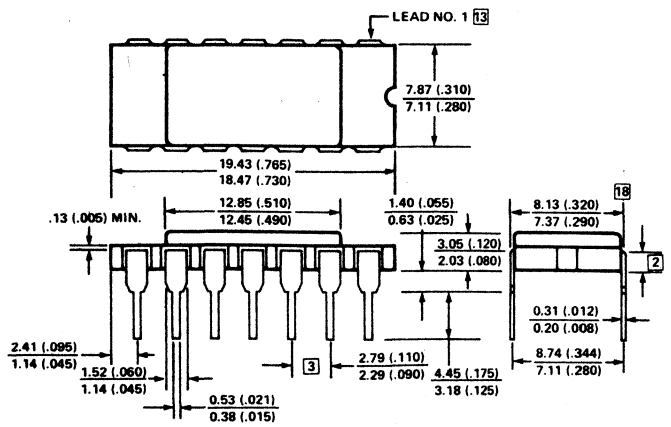
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package



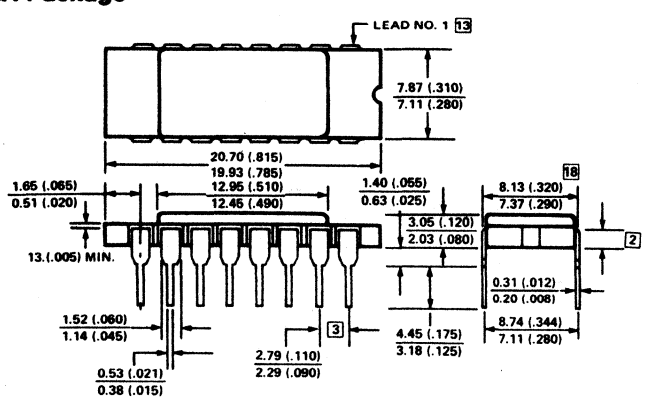
CONSTRUCTION NOTES: 10b. 11d, 12b

IHA Package



CONSTRUCTION NOTES: 10b, 11d, 12b

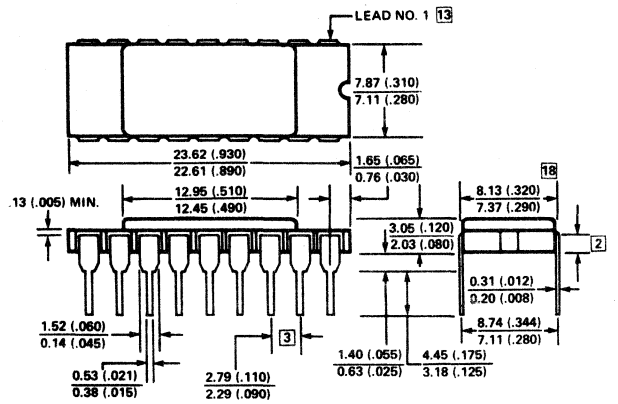
IJA Package



CONSTRUCTION NOTES: 10b, 11d, 12b

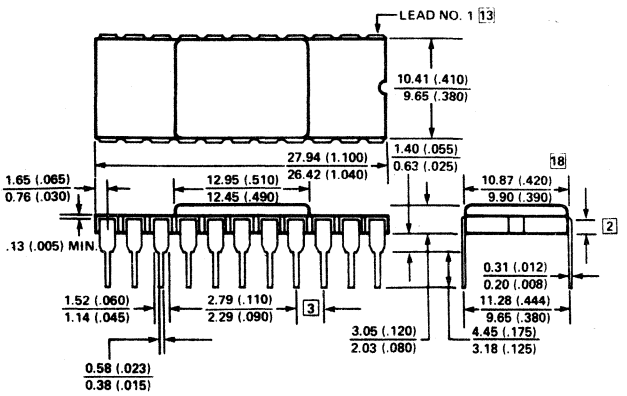
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IKA/IKB Package



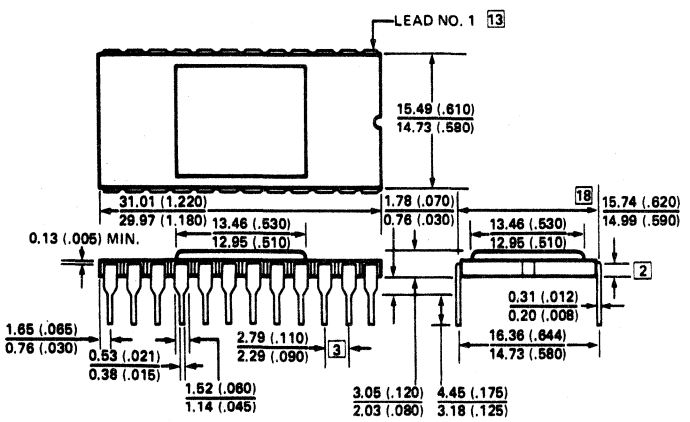
CONSTRUCTION NOTES: 10b, 11d, 12b OR 12c

IMA Package



CONSTRUCTION NOTES: 10b, 11d, 12b

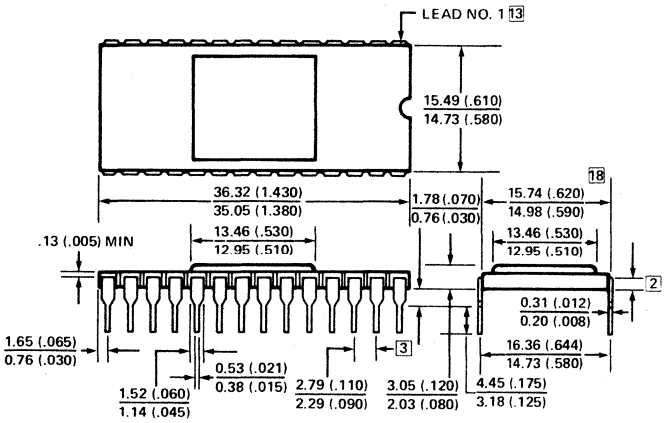
INC/INH Package



CONSTRUCTION NOTES: 10b, 11b, 12b

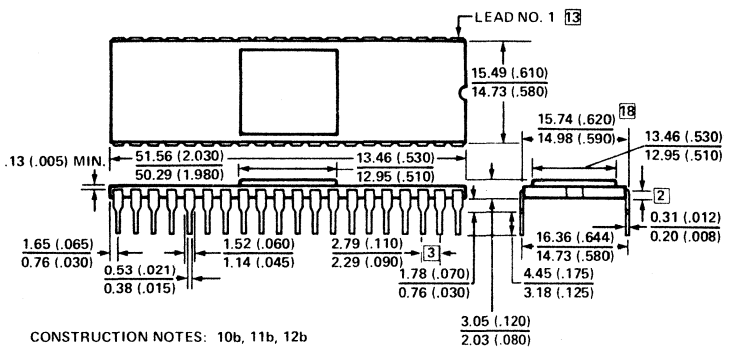
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



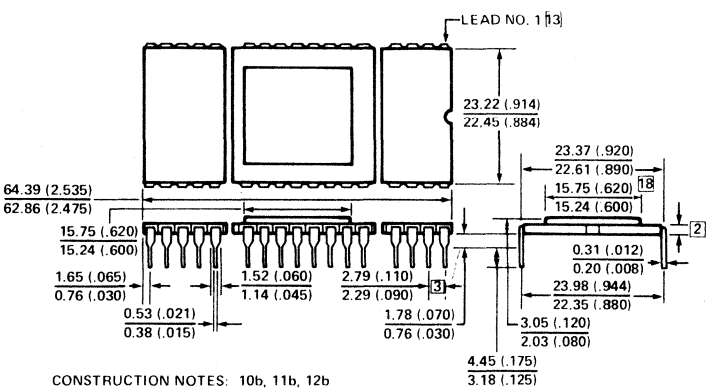
CONSTRUCTION NOTES: 10b, 11b, 12b

IWA Package



CONSTRUCTION NOTES: 10b, 11b, 12b

IZA Package



CONSTRUCTION NOTES: 10b, 11b, 12b

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